ECE 110

Professors Brunet and Loui **October 19, 2009**

HOUR EXAMINATION #2

1) Write your official (*not a nickname*):

Last Name (use capital letters): Solutions (2 versions,

First Name (use capital letters): from each professor)

NetId & UIN: ______________________________

2) Write your name and <u>section</u> at the *back* of the test

<u>DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD</u>

<u>Make sure to write your name AGAIN at the top of every page of your exam.</u>

A. Write or print clearly. Answer each problem on the exam itself. If you need extra paper, there is an extra sheet at the end of this exam. Clearly identify the problem number on any additional pages. The Boolean Algebra identities, and the decimal/binary/hexadecimal table are also attached to the exam.

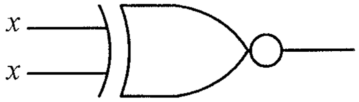
B. In order to receive partial or full credit, **you must show all your work**, e.g., your solution process, the equation(s) that you use, the values of the variables used in the equation(s), etc. **You must also include the unit of measurement in each answer.**

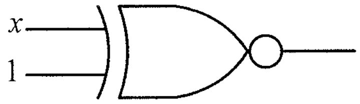
Students caught cheating on this exam will earn a grade of F for the entire course. Other penalties may include suspension and/or dismissal from the university.

loui

Problem 1 (*16 points*)

For each question, circle one answer.





1.1. The output of this XNOR gate is

(a) Always 0 (c) x

[✓ (b) Always 1] (d) x'

1.2. The output of this XNOR gate is

(a) Always 0 [✓ (c) x]

(b) Always 1 (d) x'

1.3. Among the numbers 1010_2 (binary), 101_{10} (decimal), and 10_{16} (hexadecimal), the **largest** is

(a) 1010_2 [✓ (b) 101_{10}] (c) 10_{16} (d) Insufficient information

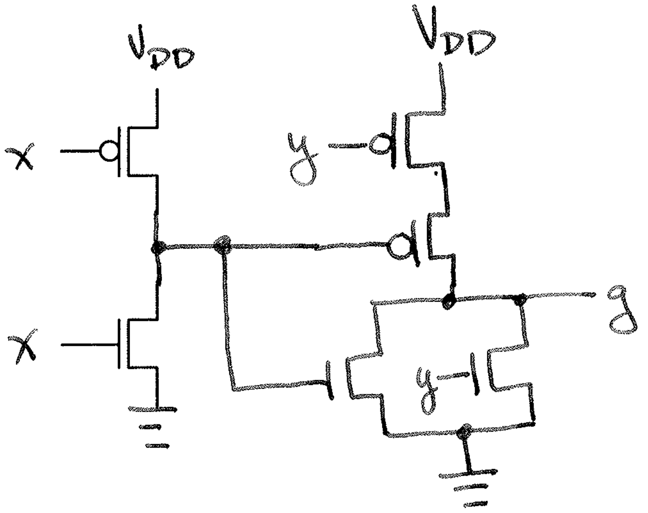
1.4. Let $u = 3B4A9E_{16}$ and $v = 60F23D_{16}$. Consider the sum $u + v$ and product $u \times v$. Then

(a) both $u + v$ and $u \times v$ are even (c) $u + v$ is even, and $u \times v$ is odd

(b) both $u + v$ and $u \times v$ are odd [✓ (d) $u + v$ is odd, and $u \times v$ is even]

Problem 2 *(9 points)*

Implement the Boolean function $g = x\,y'$ in CMOS with **six** transistors; two transistors are already given. Clearly label V_{DD} and ground, the inputs x and y, and the output g. Complemented inputs (i.e., x' and y') are not available. (Hint: since $g = (x' + y)'$, use inverter and NOR structures.)



BRUNET

Problem 1 (*16 points*)

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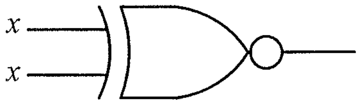

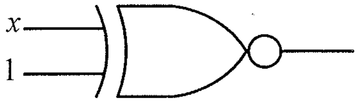

1.1. The output of this XNOR gate is

(a) Always 0 (c) x

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1.3. Among the numbers 1010_2 (binary), 101_{10} (decimal), and 10_{16} (hexadecimal), the **largest** is

(a) 1010_2 [✓ (b) 101_{10}] (c) 10_{16} (d) Insufficient information

1.4. Let $u = 3B4A9E_{16}$ and $v = 60F23D_{16}$. Consider the sum $u + v$ and product $u \times v$. Then

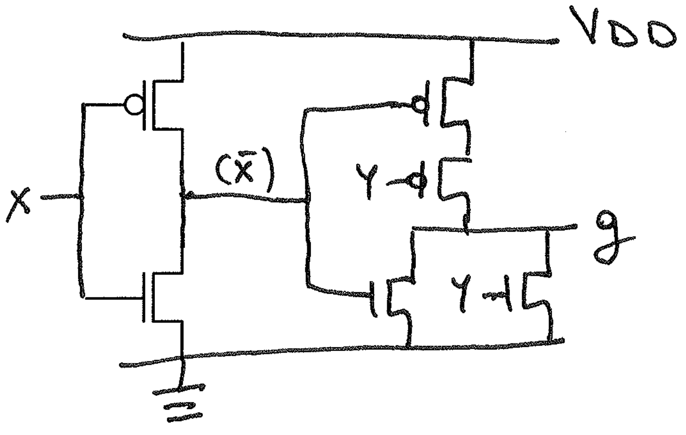
even odd

(a) both $u + v$ and $u \times v$ are even (c) $u + v$ is even, and $u \times v$ is odd

(b) both $u + v$ and $u \times v$ are odd [✓ (d) $u + v$ is odd, and $u \times v$ is even]

Problem 2 *(9 points)*

Implement the Boolean function $g = x\,y'$ in CMOS with **six** transistors; two transistors are already given. Clearly label V_{DD} and ground, the inputs x and y, and the output g. Complemented inputs (i.e., x' and y') are not available. (Hint: since $g = (x' + y)'$, use inverter and NOR structures.)



g=0 when

$\bar{x}=1$ OR Y=1

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Problem 3 *(15 points)*

The Boolean function *h* (*x*, *y*, *z*) is defined by the truth table below.

x	y	z	h
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

$$h = \bar{x}\bar{y}z + \bar{x}y\bar{z} + \bar{x}yz + x\bar{y}\bar{z} + x\bar{y}z$$

$$= \bar{x}\bar{y}z + \bar{x}y(\bar{z}+z) + x\bar{y}(\bar{z}+z)$$

(Distributivity)

$$= \bar{x}\bar{y}z + \bar{x}y\cdot 1 + x\bar{y}\cdot 1$$ (Complementarity)

$$= \bar{x}yz + \bar{x}y + x\bar{y}$$ (Identity)

(a) *(6 pts)* Find a sum-of-products (SOP) expression for *h* that has only three product terms.

$$h = \bar{x}yz + \bar{x}y + x\bar{y}$$

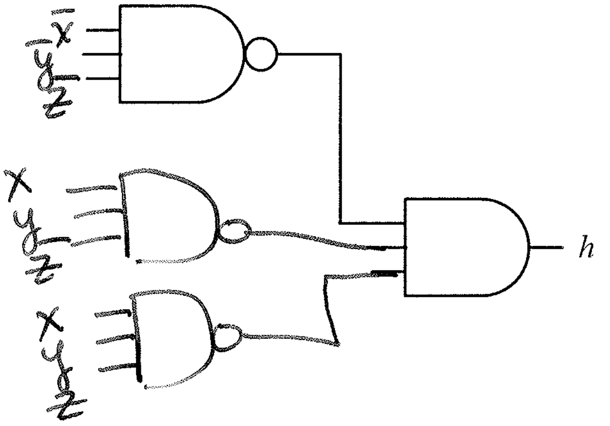
(b) *(4 pts)* Find a canonical SOP expression for the **complement** of *h*.

$h' =$ $\bar{x}\bar{y}\bar{z} + xy\bar{z} + xyz$

(c) *(5 pts)* Draw a two-level NAND-to-**AND** circuit that implements the **original** function *h*. Assume that the variables *x*, *y*, *z* and their complements *x'*, *y'*, *z'* are available as inputs. In the circuit below, you may add only NAND gates, as necessary. (Hint: use the result of part (b).)

By Involution and De Morgan,

$$h = \overline{(h')} = \overline{(\bar{x}\bar{y}\bar{z} + xy\bar{z} + xyz)} = \overline{(\bar{x}\bar{y}\bar{z})} \cdot \overline{(xy\bar{z})} \cdot \overline{(xyz)}$$



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Problem 3 *(15 points)*

The Boolean function $h(x, y, z)$ is defined by the truth table below.

x	y	z	h
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

$\bar{X}Z$

$\bar{X}Y$

$X\bar{Y}$

(a) *(6 pts)* Find a sum-of-products (SOP) expression for h that has only three product terms.

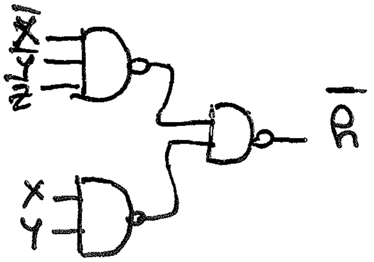
$$h = \bar{X}Y + X\bar{Y} + \bar{X}Z$$

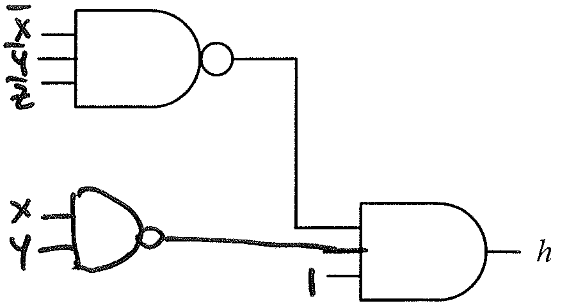
(b) *(4 pts)* Find a canonical SOP expression for the **complement** of h.

$h' =$ $\bar{X}\bar{Y}\bar{Z} + XY\bar{Z} + XYZ$

(c) *(5 pts)* Draw a two-level NAND-to-**AND** circuit that implements the **original** function h. Assume that the variables x, y, z and their complements x', y', z' are available as inputs. In the circuit below, you may add only NAND gates, as necessary. (Hint: use the result of part (b).)

$\bar{h} = \bar{X}\bar{Y}\bar{Z} + XY$ SOP ⇒ NAND-NAND





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Problem 4 *(20 points)*

Consider the Boolean function F (X, Y, Z) given by the truth table below (split in two for convenience).

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

For all Boolean expressions below, check if they are equal to F ("correct") or not ("incorrect").

☑ correct ☐ incorrect $F = \overline{X}\,\overline{Y}\,Z + \overline{X}\,Y\,Z + X\,\overline{Y}\,\overline{Z} + X\,Y\,Z + X\,\overline{Y}\,\overline{Z}$

☑ correct ☐ incorrect $F = \overline{X}\,\overline{Y}\,Z + X\,Y\,Z + X\,\overline{Y}\,\overline{Z} + \overline{X}\,Y\,Z$

☐ correct ☑ incorrect $F = \overline{X}\,\overline{Y}\,Z + X\,Y\,Z + X\,\overline{Y}\,\overline{Z}$ incorrect at 011

☐ correct ☑ incorrect $F = \overline{X}\,Y \oplus Z$ incorrect at 010, 011

☑ correct ☐ incorrect $F = \overline{\overline{X}\,\overline{Z} + Y\,\overline{Z} + X\,\overline{Y}\,Z}$

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Problem 4 *(20 points)*

Consider the Boolean function F (X, Y, Z) given by the truth table below (split in two for convenience).

X	Y	Z	F	
0	0	0	0	
0	0	1	1	$\bar{X}\bar{Y}Z$
0	1	0	0	
0	1	1	1	$\bar{X}YZ$
1	0	0	1	$X\bar{Y}\bar{Z}$
1	0	1	0	
1	1	0	0	
1	1	1	1	XYZ

For all Boolean expressions below, check if they are equal to F ("correct") or not ("incorrect").

☒ correct ☐ incorrect $F = \bar{X}\,\bar{Y}\,Z + \bar{X}\,Y\,Z + X\,\bar{Y}\,\bar{Z} + X\,Y\,Z + X\,\bar{Y}\,\bar{Z}$ same

☒ correct ☐ incorrect $F = \bar{X}\,\bar{Y}\,Z + X\,Y\,Z + X\,\bar{Y}\,\bar{Z} + \bar{X}\,Y\,Z$

☐ correct ☒ incorrect $F = \bar{X}\,\bar{Y}\,Z + X\,Y\,Z + X\,\bar{Y}\,\bar{Z}$ missing minterm $\bar{X}YZ$

☐ correct ☒ incorrect $F = \bar{X}\,Y \oplus Z = \underbrace{\bar{X}Y\bar{Z}}_{\text{incorrect}} + \overline{\bar{X}Y}\,.Z$

☒ correct ☐ incorrect $F = \overline{\bar{X}\,\bar{Z} + Y\,\bar{Z} + X\,\bar{Y}\,Z}$

$\bar{X}\bar{Z} + Y\bar{Z} + X\bar{Y}Z$ is equal to 1 whenever $F=0$.

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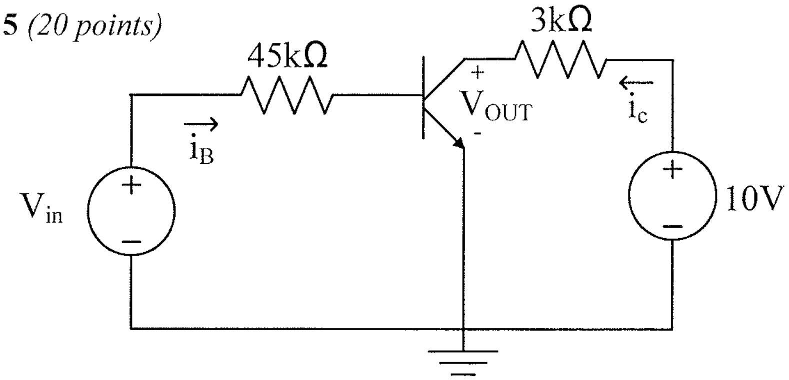
Problem 5 *(20 points)*



$V_{BEON} = 0.6V$
$V_{CESAT} = 0.2V$
$\beta = 80$

For all cases below, cross out any incorrect answer, and provide an explanation and the **correct** answers (there may be rows for which all answers are correct, and no explanation is necessary; there may be rows for which more than one answer is incorrect). V_{in} is given (and correct). Two significant digits after the decimal point are used for all numerical values.

V_{in} (volts)	i_B (μA)	i_C (mA)	V_{OUT} (volts)	Explanation
2	31.11	~~3.11~~ 2.49	~~0.67~~ 2.53	Transistor is active. $i_c = \beta i_B = 80 \times 31.11 \mu A = 2.49 mA$ $V_{out} = 10 - 3k \times i_c = 2.53 V$
1	8.89	0.71	7.87	All correct
0.5	~~-2.22~~ 0	~~-0.18~~ 0	10	Transistor is off since $V_{in} < V_{BEON}$. So $i_B = i_c = 0$
3	53.33	~~4.27~~ 3.27	0.2	At saturation, $V_{OUT} = V_{CESAT} = 0.2V$ and $i_c = \frac{10 - V_{OUT}}{3k} = 3.27 mA$ So $i_c < \beta i_B = 4.27 mA$

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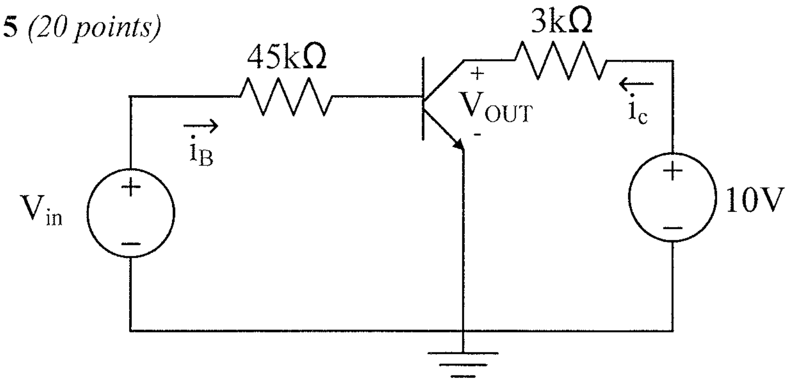
Problem 5 *(20 points)*



$V_{BEON} = 0.6V$
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V_{in} (volts)	i_B (μA)	i_C (mA)	V_{OUT} (volts)	Explanation
2	31.11	~~3.11~~ 2.49	~~0.67~~ 2.53	$i_C \neq 100\, i_B$; $\beta = 80$. $i_C = 31.11 \mu A \times 80 = 2.49 mA$ $V_{out} = 10 - 3k\, i_C = 2.53$
1	8.89	0.71	7.87	All correct. BJT is active
0.5	~~-2.22~~ 0	~~-0.18~~ 0	10	$0.5 < V_{BEON} \Rightarrow$ off $i_B = i_C = 0$
3	53.33	~~4.27~~ 3.27	0.2	BJT is saturated $i_C \neq 80\, i_B$ $i_C = \frac{10 - 0.2}{3k} = 3.27 mA$

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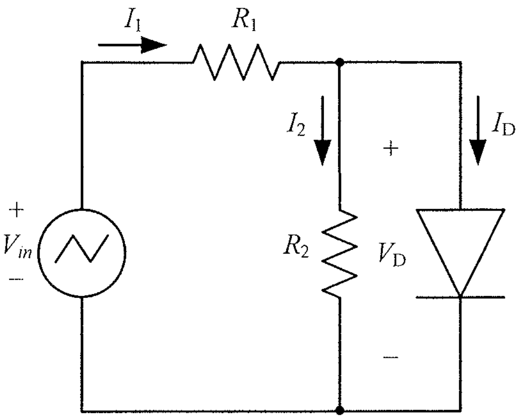
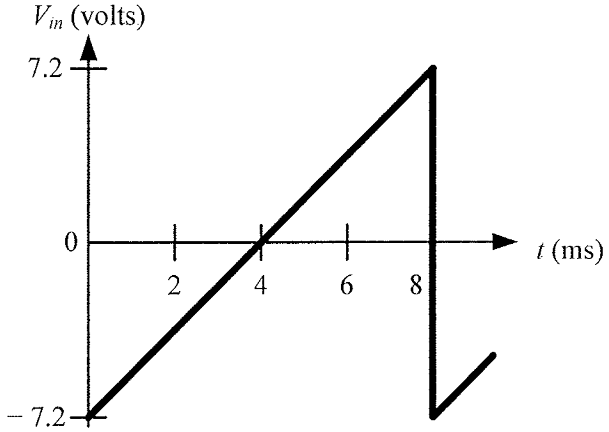
Problem 6. (*20 points*)

The circuit below has a sawtooth wave voltage source V_{in} whose period is 8 ms, a diode with $V_{on} = 0.6$ V, and resistors $R_1 = 4$ kΩ and $R_2 = 2$ kΩ. From $t = 0$ to $t = 8$ ms, $V_{in} = 1.8\,t - 7.2$ volts. By KCL, $I_1 = I_2 + I_D$. By KVL and Ohm's Law, $V_{in} = V_D + I_1R_1$, and $V_D = I_2R_2$. To analyze this circuit, use the **large signal model**.





(a) (*6 pts*) Show that the diode is **on** when $V_{in} > 1.8$ V. **Explain your reasoning**.

(b) (*6 pts*) Show that $V_D = V_{in}/3$ when the diode is **off. Explain your reasoning**.

Diode is on when $V_D = 0.6$ and $I_D > 0$.

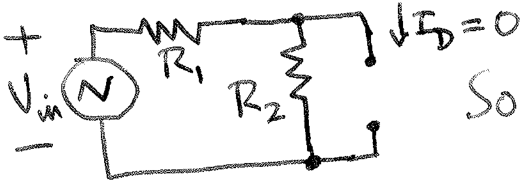
$$I_D = I_1 - I_2 = \frac{V_{in} - V_D}{R_1} - \frac{V_D}{R_2} > 0$$

when $\frac{V_{in} - V_D}{R_1} > \frac{V_D}{R_2}$

$$V_{in} > V_D + \frac{R_1 V_D}{R_2} = 0.6 + \frac{4k}{2k}0.6$$

$$= 0.6 + 1.2 = 1.8 \text{ V}$$

When the diode is off, it is essentially an open



So by VDR,

$$V_D = \frac{R_2 V_{in}}{R_1 + R_2} = \frac{2k}{4k+2k} V_{in} = V_{in}/3$$

(c) (*8 pts*) Plot the voltage V_D for one period. Label the vertical axis with the voltages, and the horizontal axis with the times, at which the behavior of the circuit changes. **Explain your reasoning.**

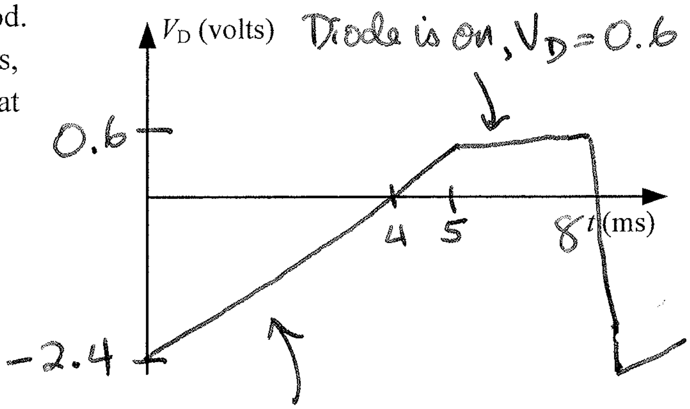
Diode is on (by part (a)) when $V_{in} > 1.8$, when

$1.8t - 7.2 > 1.8$

$1.8t > 7.2 + 1.8 = 9.0$

$t > 5$

At $t=0$, $V_D = \frac{-7.2}{3} = -2.4$



Diode is on, $V_D = 0.6$

Diode is off, $V_D = V_{in}/3$ (by part (b))

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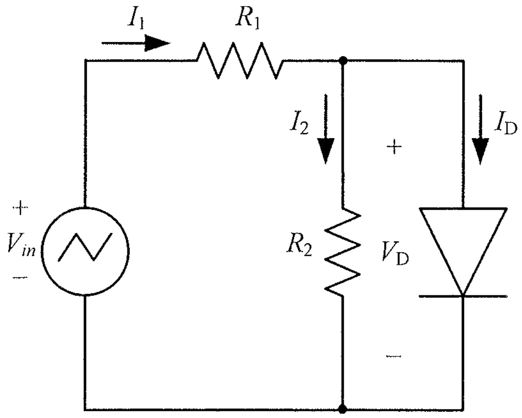
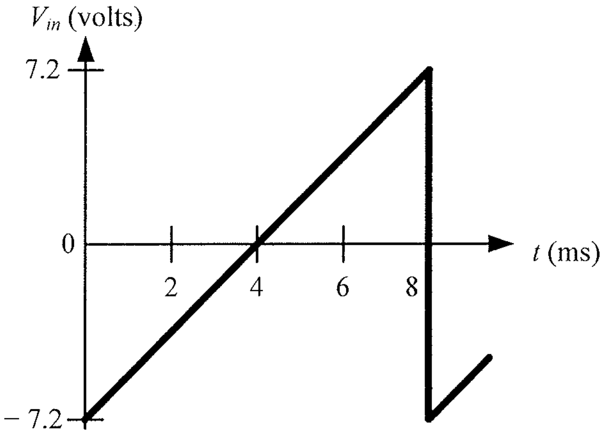
Problem 6. *(20 points)*

The circuit below has a sawtooth wave voltage source V_{in} whose period is 8 ms, a diode with $V_{on} = 0.6$ V, and resistors $R_1 = 4$ kΩ and $R_2 = 2$ kΩ. From $t = 0$ to $t = 8$ ms, $V_{in} = 1.8\,t - 7.2$ volts. By KCL, $I_1 = I_2 + I_D$. By KVL and Ohm's Law, $V_{in} = V_D + I_1R_1$, and $V_D = I_2R_2$. To analyze this circuit, use the **large signal model**.





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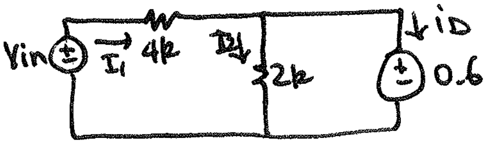


$I_2 = \frac{0.6}{2k}$ $I_1 = \frac{Vin - 0.6}{4k}$

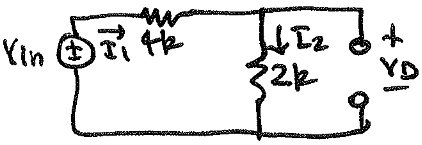
$i_D = I_1 - I_2 = \frac{Vin - 0.6}{4k} - \frac{0.6}{2k}$

diode is on : $i_D > 0$?

$\Rightarrow \frac{Vin - 0.6}{4k} > \frac{0.6}{2k}$

$\Rightarrow Vin > 2 \times 0.6 + 0.6 \; (= 1.8)$

(b) *(6 pts)* Show that $V_D = V_{in}/3$ when the diode is **off. Explain your reasoning**.

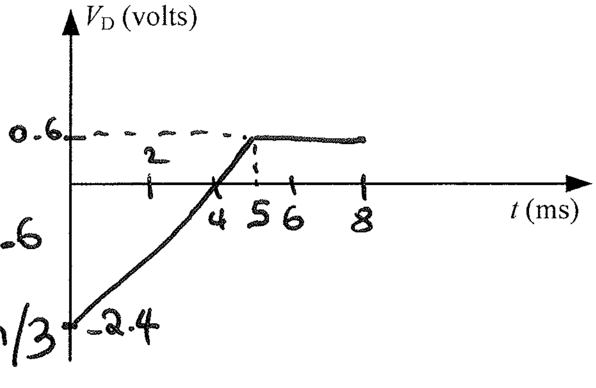


$I_1 = I_2$ by the VDR:

$V_D = \frac{2k}{4k + 2k} Vin = \frac{2}{6} Vin$

$\Rightarrow V_D = Vin/3$

(c) *(8 pts)* Plot the voltage V_D for one period. Label the vertical axis with the voltages, and the horizontal axis with the times, at which the behavior of the circuit changes. **Explain your reasoning.**



$Vin > 1.8$ diode is on : $V_D = 0.6$

$Vin < 1.8$ diode is off : $V_D = Vin/3$

$Vin = 1.8$ at $t = 5$ ms