

HOUR EXAMINATION #2

Last Name (use capital letters): _____
First Name (use capital letters): _____
Signature: Solution

Circle your section: AL1(1pm)-Trick

BL1(noon)-Brunet

DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD

Problem	Value	Score
1	20	
2	20	
3	20	
4	20	
5	20	
Total	100	

A. Write or print clearly. Answer each problem on the exam itself. If you need extra paper, there is an extra sheet at the end of this exam. Clearly identify the problem number on any additional pages. The Boolean Algebra identities are also given at the end of the exam.

B. In order to receive partial or full credit, you must show all your work, e.g., your solution process, the equation(s) that you use, the values of the variables used in the equation(s), etc. You must also include the unit of measurement in each answer.

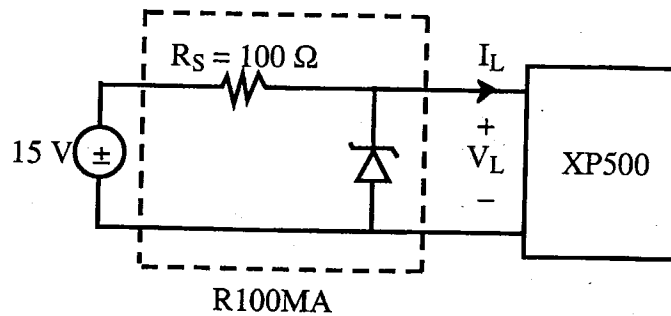
Students caught cheating on this exam will earn a grade of F for the entire course. Other penalties may include suspension and/or dismissal from the university.

Problem 1 (20 points)

Alex is using a 15 V voltage source and a R100MA voltage regulator with a 5 V, 2 W Zener diode to power the XP500 circuit which is rated at 5 V and 200 mA.

Unfortunately, Alex finds that under maximum load conditions $V_L = 3$ V.

Advise Alex how he can modify the R100MA circuit so that it will supply a constant 5 V to the XP500 circuit over the current range $0 \leq I_L < 200$ mA.



Voltage regulator requirement: I_S

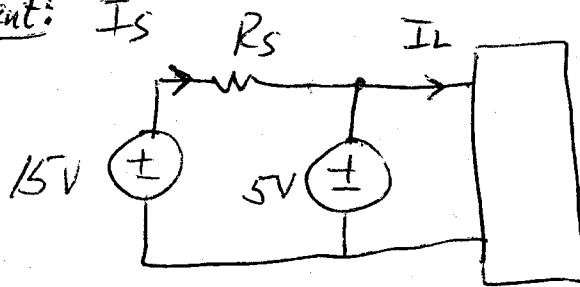
$$I_S = \frac{15V - 5V}{R_S} \geq I_{LMAX}$$

Given:

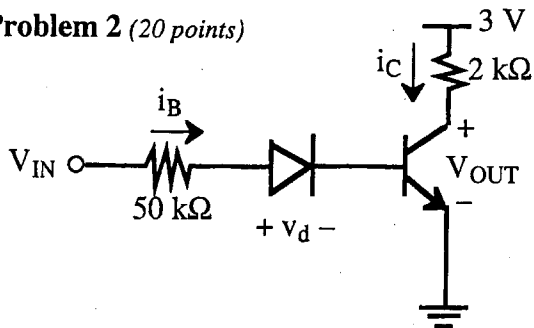
$$I_{LMAX} = 200mA,$$

so

$$R_S \leq \frac{10V}{.2A} = \underline{50\Omega}$$



Problem 2 (20 points)



Assume:

$$\beta = 100$$

$$V_{ON} = V_{BEON} = 0.7 \text{ V}$$

$$V_{CESAT} = 0.2 \text{ V}$$

$$V_{IN} = 1.5 + 0.5 \sin \omega t$$

Show **all** of your work for all parts.

a) (2 pts.) Give the range of values for V_{IN} :

$$1.0 \leq V_{IN} \leq 2.0$$

b) (9 pts.) For the given V_{IN} explore all possible states of the BJT in the circuit. If a state is possible, give the range of V_{IN} values for that state (if not, check "not possible").

State of BJT	not possible	possible, range of V_{IN}
OFF	<input type="checkbox"/>	$1.0 \leq V_{IN} \leq 1.4 \text{ V}$
ACTIVE	<input type="checkbox"/>	$(V_{MIN}) 1.4 \text{ V} \leq V_{IN} \leq 2.0 \text{ V} (V_{MAX})$
SATURATED	<input checked="" type="checkbox"/>	$\leq V_{IN} \leq$

$$I_{C MAX} = \frac{3\text{V} - 0.2\text{V}}{2\text{k}\Omega} = 1.4\text{mA}, \quad I_B = \frac{1.4\text{mA}}{100} = 14\text{ }\mu\text{A}$$

$$V_{iH} = 1.4\text{V} + (14\text{ }\mu\text{A})(50\text{k}\Omega) = 2.1\text{V}$$

c) (9 pts.) Compute the values of i_B , i_C , and V_{OUT} when the BJT is active and for the extreme values of V_{IN} (i.e., for V_{MIN} and V_{MAX}) found in b).

V_{IN}	i_B (μA)	i_C (mA)	V_{OUT} (volts)
$V_{MIN} = 1.4\text{V}$	0	0	3
$V_{MAX} = 2.0\text{V}$	12	1.2	0.6

$$i_B = \frac{V_{IN} - 1.4\text{V}}{50\text{k}\Omega}, \quad i_C = \beta i_B$$

$$V_{out} = 3\text{V} - (2\text{k}\Omega) i_C$$

Problem 3 (20 points)

- a) Convert the Boolean function $F = \overline{\overline{XY} \cdot \overline{X} \overline{Y}}$ to a SOP form. State the identity or method you used in the conversion.

(4pts) De Morgan's Identity yields

$$F = XY + \overline{X} \overline{Y}$$

- b) Complete the truth table for the Boolean function in part 3a).

(4pts) $F = 1$ for X and $Y = 1$
 or
 $F = 1$ for \overline{X} and $\overline{Y} = 1$
 $\Rightarrow X$ and $Y = 0$

X	Y	F
0	0	1
0	1	0
1	0	0
1	1	1

- c) For the given truth table, write a Boolean function for it in canonical SOP form.

X	Y	Z	G
0	0	0	1 $\overline{X} \overline{Y} \overline{Z}$
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1 $X \overline{Y} \overline{Z}$
1	0	1	1 $X \overline{Y} Z$
1	1	0	0
1	1	1	0

(6pts)
$$F = \overline{X} \overline{Y} \overline{Z} + X \overline{Y} \overline{Z} + X \overline{Y} Z$$

- d) Find the optimal SOP Boolean function for the truth table in 3c).

HINT: The optimal corresponding circuit has 3 gates and ~~4 gates~~. Show your work. each gate has 2 inputs

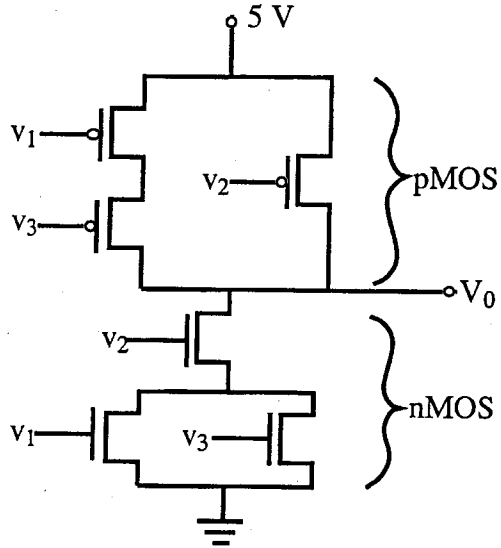
(6pts)
$$F = \overline{X} \overline{Y} \overline{Z} + X \overline{Y} \overline{Z} + X \overline{Y} Z + X \overline{Y} Z$$

$$= (\overline{X} + X) \overline{Y} \overline{Z} + X \overline{Y} (\overline{Z} + Z) = \overline{Y} \overline{Z} + X \overline{Y}$$

Problem 4 (20 points)

a) (10 pts.) Complete the truth table for the CMOS circuit below. A low voltage is a logic "0" and a high voltage is a logic "1."

V_1	V_2	V_3	V_0
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



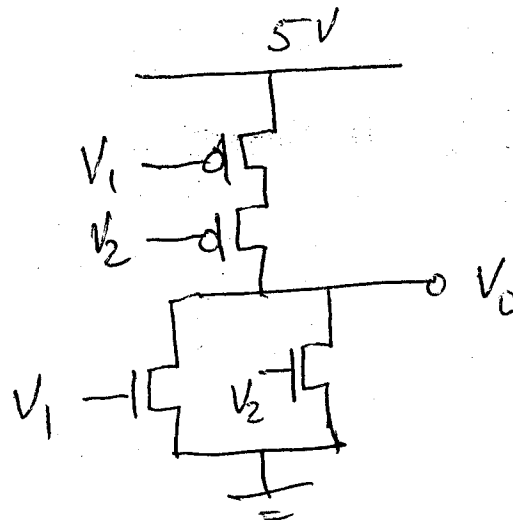
$$\bar{V}_0 = V_2 (V_1 + V_3)$$

b) (10 pts.) For the given truth table, draw the CMOS circuit that implements the logic function specified by the truth table below.

V_1	V_2	V_0
0	0	1
0	1	0
1	0	0
1	1	0

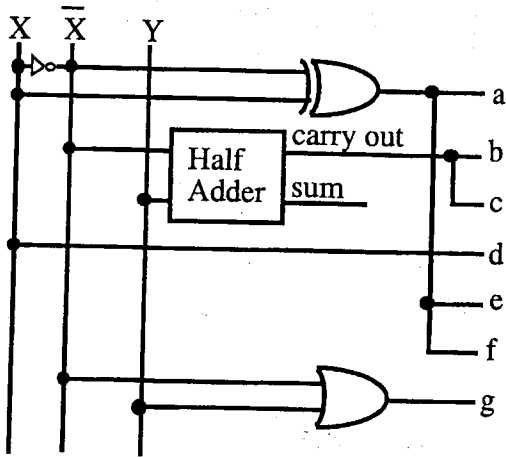
$$V_0 = \bar{V}_1 \bar{V}_2$$

$$\bar{V}_0 = \overline{\bar{V}_1 \bar{V}_2} = V_1 + V_2$$



Problem 5 (20 points)

a) (12 pts.) Fill in the truth tables for the circuit below. Show your work.



X	Y	a	b	c	d	e	f	g
0	0	1	0	0	0	1	1	1
0	1	1	1	1	0	1	1	1
1	0	1	0	0	1	1	1	0
1	1	1	0	0	1	1	1	1

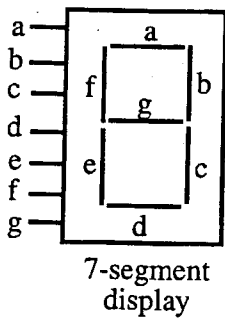
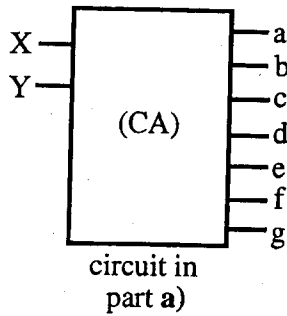
$$a = e = f = \bar{X} \oplus X = 1$$

$$b = c = \bar{X} Y$$

$$d = X$$

$$g = \bar{X} + Y$$

b) (8 pts.) The circuit in part a) and four 7-segment displays are used to produce a 4-character display.



0 0	0 1	1 0	1 1
X Y (CA)	X Y (CA)	X Y (CA)	X Y (CA)
display 1	display 2	display 3	display 4
$a=e=f=g=1$	$a=b=c=e=f$	$a=d=e=f=1$	$a=d=e=f=g=1$
• Draw what is displayed: $=g=1$			
• State what is displayed:			