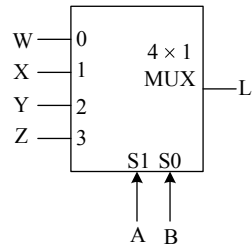
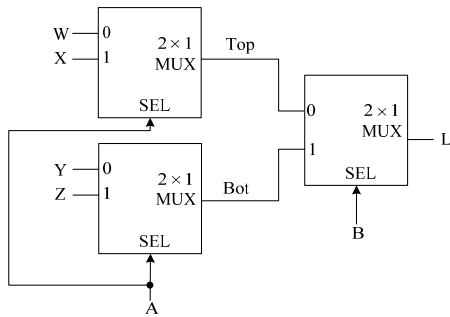


Problem 1 (10 points)

Sam was asked to design the 4×1 MUX below using three 2×1 MUXs.



Sam suggested the following circuit:



a) [7 pts.] Check Sam's design. Fill out the table below for Sam's circuit.

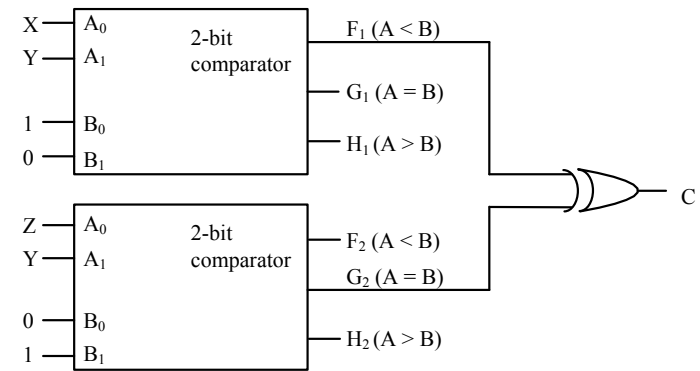
A	B	Top	Bot	L
0	0			
0	1			
1	0			
1	1			

b) [3 pts.] Is Sam's circuit correctly implementing the 4×1 MUX?

Yes No

Justify answer:

Problem 7 (20 points)



a) (15 pts.) Fill in the table below for the circuit above.

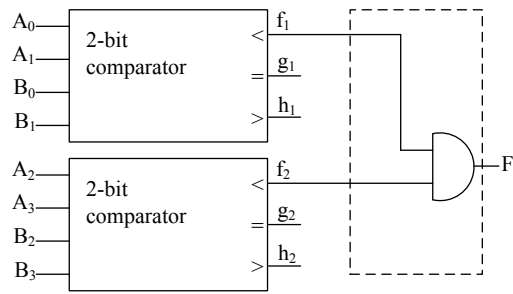
X Y Z	F ₁	G ₁	F ₂	G ₂	C
0 0 0					
0 0 1					
0 1 0					
0 1 1					
1 0 0					
1 0 1					
1 1 0					
1 1 1					

b) (5 pts.) Deduce a canonical SOP for output C.

$C(X, Y, Z) =$

Problem 4 (20 points)

Sam designed a 4-bit comparator (below) for output F ($A < B$): $F = 1$ when $(A_3A_2A_1A_0)_2 < (B_3B_2B_1B_0)_2$.

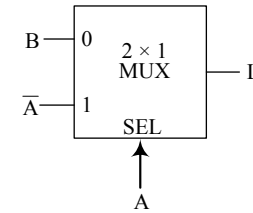


Sam's design ($F = f_1 \cdot f_2$) is incomplete and not optimal. Improve the design (replace circuit in dotted box). Provide a correct design with a minimum number of gates. No need to draw the circuit! You must completely justify your design and provide a Boolean expression for F .

$F =$

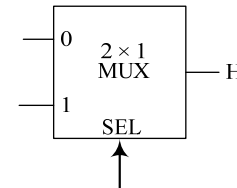
Problem 1 [15 points]

(a) [10 pts.] The circuit below implements the F output of a 1-bit comparator ($F = 1$ when $A < B$).

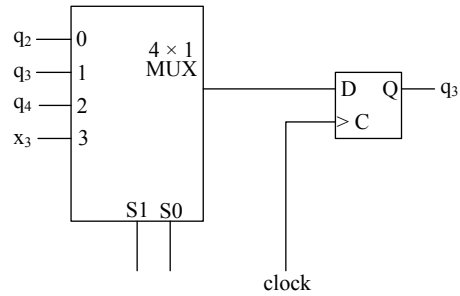


Provide the truth table for L (make sure you explain how you found it) and show that $L = F$ indeed.

(b) [5 pts.] Implement the H output of a 1-bit comparator ($A > B$) using the MUX below. Give the truth table for H .



Problem 1 (16 points) A 5-bit register with state $q_4q_3q_2q_1q_0$ is implemented with D flip-flops and 4×1 multiplexers. Here is part of the circuit for bit position 3 in the register.



The register has three control signals L (Load), H (sHift), and R (diRection).
 If $L = 1$, then the external input $x_4x_3x_2x_1x_0$ is loaded into the register.
 If $L = 0$ and $H = 0$, then there is no change to the register state.
 If $L = 0$ and $H = 1$ and $R = 0$, then the register contents shift left.
 If $L = 0$ and $H = 1$ and $R = 1$, then the register contents shift right.

Determine the multiplexer inputs $S1$ and $S0$ as a function of L , H , and R . Explain your reasoning.

L	H	R	$S1$	$S0$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Problem 6 (20 points) The sequential network below has two positive-edge-triggered D flip-flops that share a common clock. There is one external input signal x .

- a) [8 pts.] Complete the table to show the values of d_a and d_b as functions of q_a , q_b , and x .
- b) [12 pts.] Complete the timing diagram to show the waveforms for d_a , d_b , q_a , q_b . Initially $q_a = q_b = 0$. Assume that the delays in the gates and in the multiplexer are negligible.

q_a	q_b	x	d_a	d_b
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

