ECE 199 Exam 1 Fall 2002

Tuesday, September 24th, 2002

Name:

- **Be sure your exam booklet has 8 pages.**
- **Write your name at the top of each page.**
- **This is a closed book exam.**
- **You are allowed one 8.5 x 11 sheet of notes.**
- **Absolutely no interaction between students is allowed.**
- **Show all of your work.**
- **Challenge questions are marked with a *****
- **Don't panic, and good luck!**

Problem 1	20 points	_____
Problem 2	20 points	_____
Problem 3	20 points	_____
Problem 4	20 points	_____
Problem 5	20 points	_____
Total	100 points	_____

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Problem 1 (20 points): Short Answer

Answer the following questions with a **very brief and precise** statement. A long statement is a good indication that your response will be marked incorrect. As a general guideline, each correct response should require no more than 20 words.

Part A (7 points): What range of values can be represented with a 2's complement integer consisting of 10 bits?

Part B (7 points): If the total size of memory is 1MB (2^{20} Bytes), and its addressability is 32 bytes, how many bits of address are required to address all of memory?

Part C (6 points): Say we have an ISA using 32-bit instructions and memory is byte addressable, by how much must we increment the PC after fetching an instruction?

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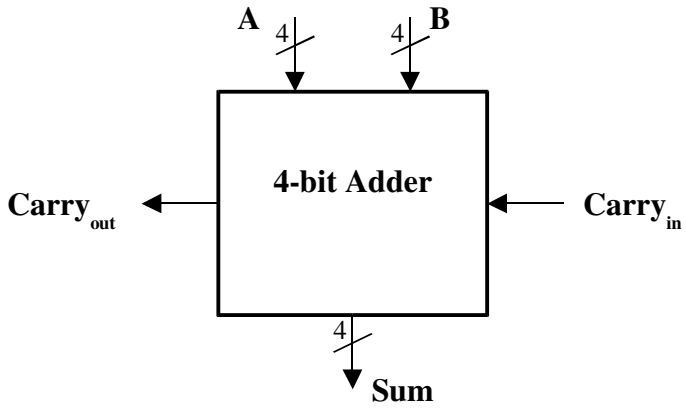
Problem 2 (20 points): Design using components.

Part A (8 points): Say we have at our disposal a 4-bit adder, such as the one in the diagram below. The adder is able to add two 4-bit numbers, **A** and **B**, along with a $\mathbf{Carry_{in}}$, and generate a 4-bit **Sum** along with a $\mathbf{Carry_{out}}$. We'd like to use the adder to create a **left-shifter** (which is a very useful logic element in digital systems design). As the name implies, the left-shifter shifts the input bit pattern by one bit position to the left. The left-shifter takes two inputs: **Q**, the 4-bit value to be shifted, and $\mathbf{S_{in}}$, a single bit that fills the vacated bit position of **Q**. The outputs of the shifter are **P**, which is defined as $\mathbf{Q_2Q_1Q_0S_{in}}$, and $\mathbf{S_{out}}$, which will be $\mathbf{Q_3}$.

Using only the 4-bit adder as a component, create a left-shifter.



Part B (8 Points): Using as many 4-bit adders as you need, create a left-shifter that shifts a 16-bit value left by one bit.

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Problem 2, continued:

***Part C** (4 points): Using as many 4-bit left-shifters and 4-bit adders as you need, create a 4-bit right-shifter. The right-shifter works exactly like a left shifter except it shifts the input **A** one bit position to the right.

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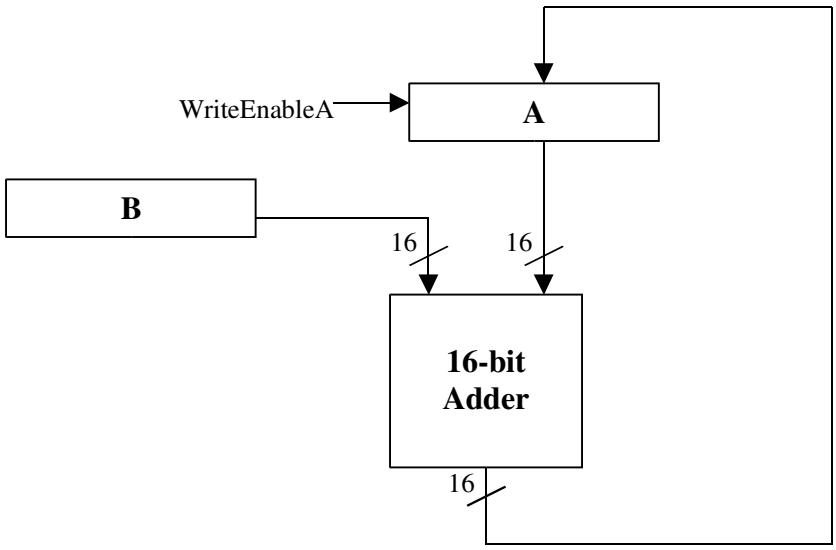
Problem 3 (20 points): Logic Analysis

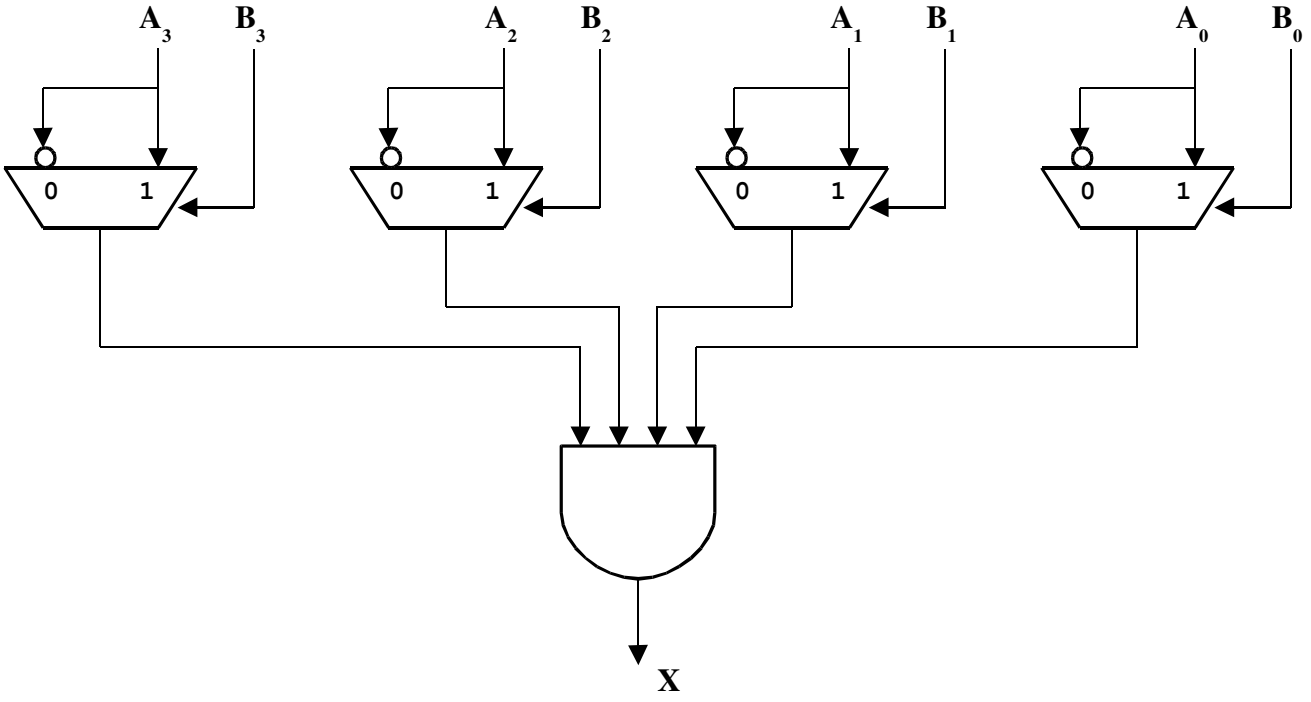
Part A (10 points): In the logic diagram below, **A** and **B** are both 16-bit registers connected to a 16-bit adder. Assume that register **A** starts off with a value of 0 and register **B** has the value *X*.

What will **A** contain after **WriteEnableA** is asserted *5* times?

What will be calculated if **WriteEnableA** is asserted *N* times?



Part B (10 points): For the following logic diagram, what does a 1 on the output **X** indicate? A correct answer should require no more than 10 words.



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Problem 4 (20 Points): Memory

For this problem, consider the 2^3x3 bit memory provided below. The memory contains the values shown.

101	000
001	001
011	010
111	011
110	100
010	101
000	110
100	111

Part A (10 points): If we implemented this memory like the logic diagram of memory shown in class, how many gated D latches would be required? Do not include the MAR and MDR.

Part B (10 points): Assume that we start reading this memory at location 000. Each value read from memory will be treated as the address of the next read. That is, if we read an A from the current location, then we will read memory location A next. If we read a total of 8 memory locations, what is the stream of values read from memory?

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Problem 5 (20 Points): The von Neumann Model

For this question, refer to the LC-2 version of the von Neumann Model below. The LC-2 is about to perform an instruction **FETCH**.

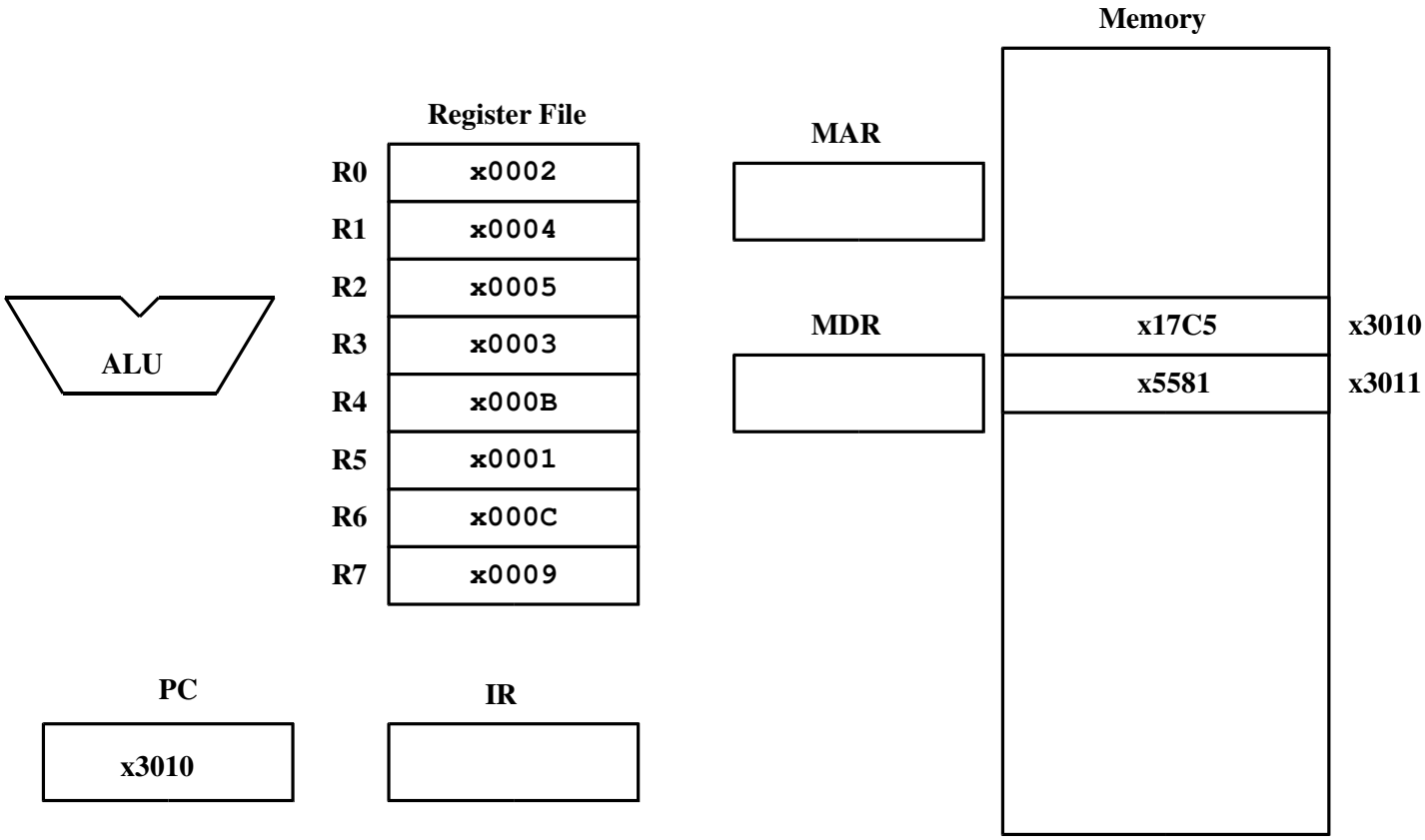
Say the LC-2 completes the execution of two instructions (i.e., the instruction cycle is performed twice). Clearly denote the final values in the diagram below.

Part A (10 points): Register File

Part B (5 points): PC and IR

Part C (5 points): MAR and MDR

Hint: The instruction in x3010 is an ADD instruction and the instruction in x3011 is an AND.



Name:

Scratch Paper for Calculations