

ECE 199 Exam 1 Fall 2003

Tuesday, September 30th, 2003

Name:

- **Be sure your exam booklet has 11 pages.**
- **Write your name at the top of each page.**
- **This is a closed book exam.**
- **You are allowed one 8.5 x 11 sheet of notes.**
- **Absolutely no interaction between students is allowed.**
- **Show all of your work.**
- **Challenge questions are marked with a *****
- **Don't panic, and good luck!**

Problem 1	20 points	_____
Problem 2	20 points	_____
Problem 3	20 points	_____
Problem 4	20 points	_____
Problem 5	20 points	_____
Total	100 points	_____

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Problem 1 (20 points): Short Answer

Part A (12 points): How many bits are necessary to store a single number in the range 0 to 99999...

a) (4 points) ...using an unsigned representation?

b) (4 points) ...using a 2's complement representation?

c) (4 points) ...using ASCII?

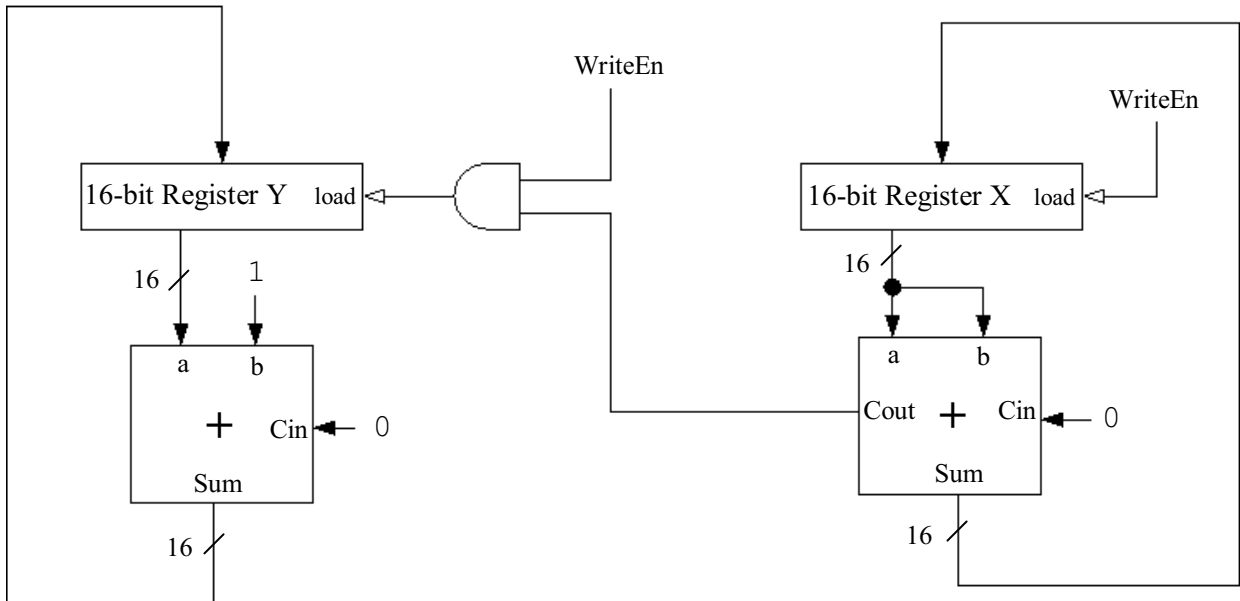
Part B (4 points): Explain one advantage of a floating-point representation over a 2's complement representation.

Part C (4 points): Prove that the functions OR and NOT together are logically complete.

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Problem 2 (20 Points): Sequential Circuits

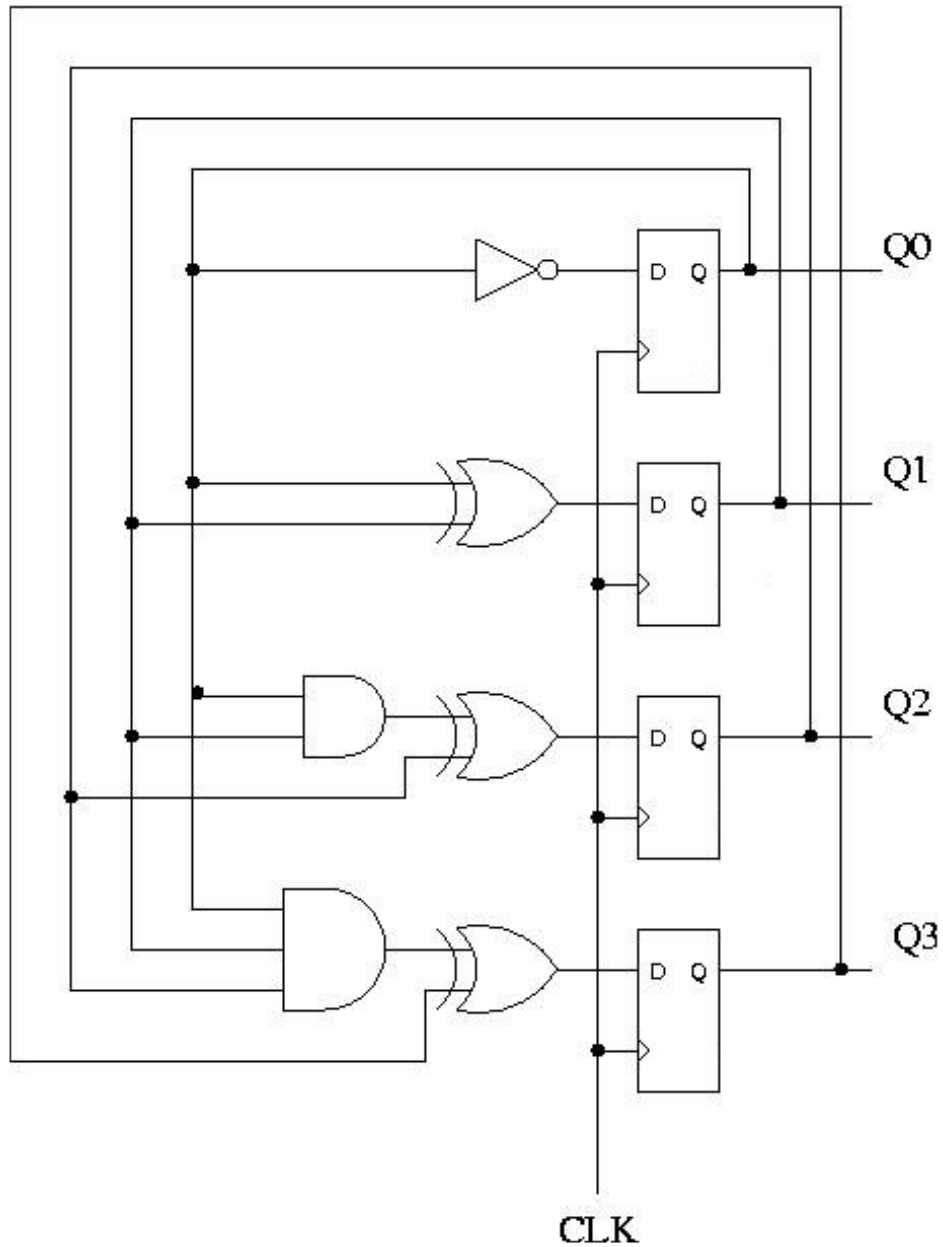
Part A (10 points): For the diagram below, assume that Y initially contains a 0 while X contains some 2's complement number. In a single sentence, describe what the contents of Y represent after the WriteEn signal is raised to a logical '1' and lowered to '0' 16 times.



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Problem 2, continued:

Part B (10 points): Describe what the following sequential circuit does in a sentence. Assume that the output $Q_3Q_2Q_1Q_0$ is initially 0000.



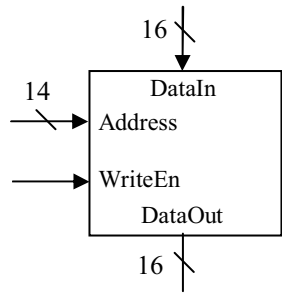
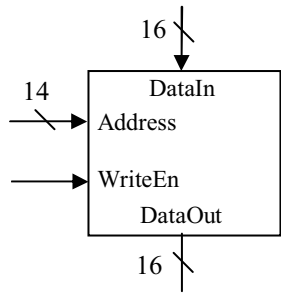
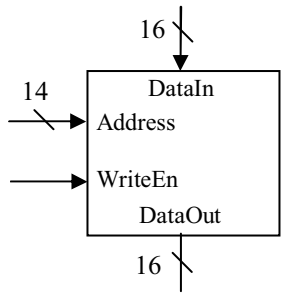
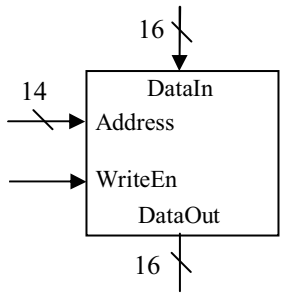
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Problem 3 (20 Points): Memories

Part A (4 points): A memory stores a total of 16 Mbits (1 Mbit is 2^{20} bits) and uses 19-bit addresses. What is the addressability of this memory in bits?

Part B (4 points): Is it ever possible to have the PC, IR, MAR, and MDR all contain the same value during the FETCH cycle of the von Neumann instruction cycle? If so, explain how. If not, explain why not.

*****Part C (12 points):** You must design a 2^{16} by 16-bit memory for the LC-3. However, you have only been given four 2^{14} by 16-bit memory blocks to work with. Draw your design on the next page, using any gates or combinational logic blocks we discussed in class in addition to the 4 memory blocks.

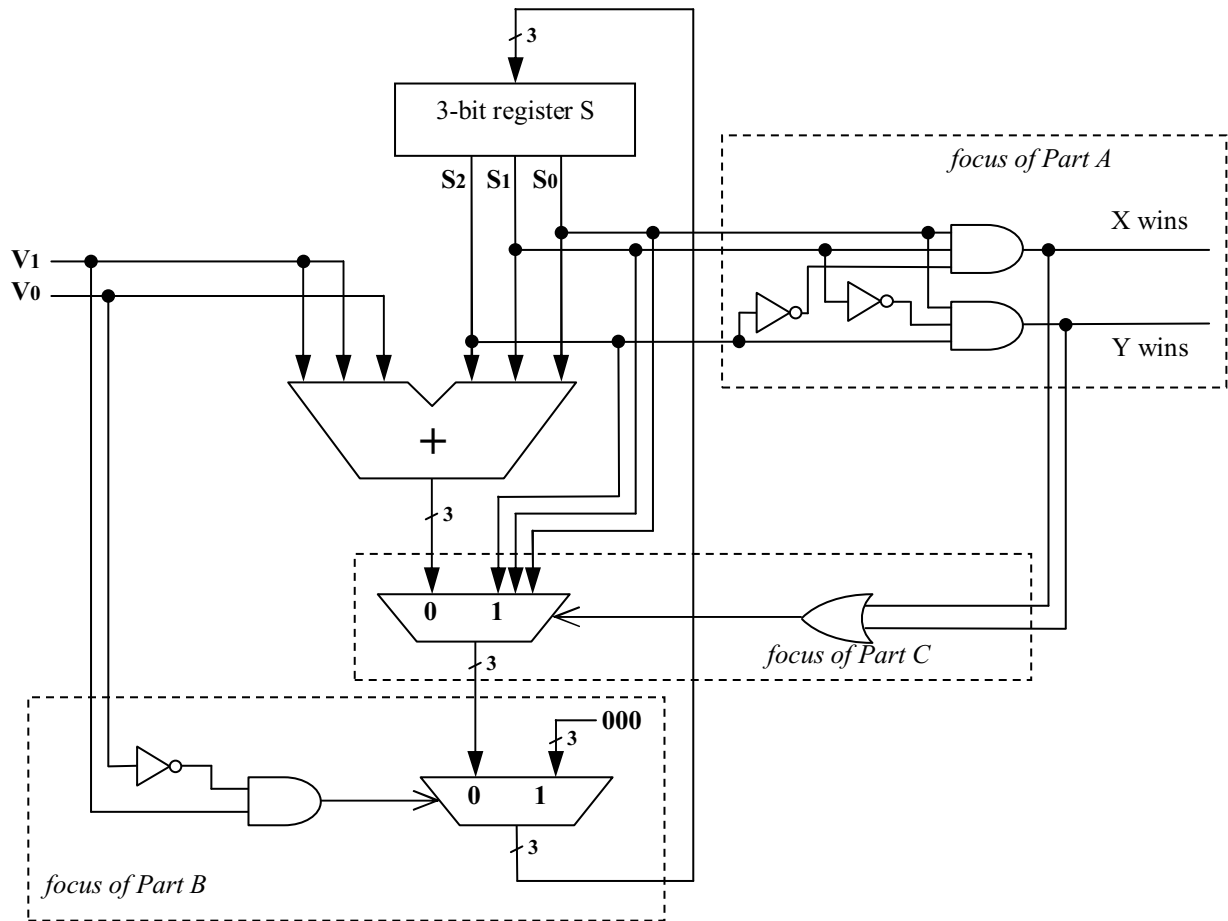


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Problem 4 (20 Points): Finite State Machines

A certain finite state machine implements a match scoring system for a game played in rounds by two players (X and Y). Each round can result in a win for X, a win for Y, or a tie. When a player gets ahead by three rounds (has won three more times than the other player), that player wins the match. Answer all parts of this question based on the implementation shown below. The parts are designed to help you through the analysis.



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Problem 4, continued:

Part A (2 points): For what value(s) of the register S does player X win? Player Y?

Part B (3 points): Explain the function of the bottom mux and the logic controlling it.

Part C (3 points): Explain the function of the OR gate and the mux that it controls.

Part D (4 points): Explain the meaning of the bits held in register S.

Part E (4 points): Fill in the table below of input values and their meanings; three of the meanings have been given already.

V_1	V_0	meaning
		player X won a round
		player Y won a round
		round tied
		(your answer to Part B)

*****Part F** (4 points) How many bits of state are necessary if the game is instead played until one player has won three times? Justify your answer.

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Problem 5 (20 Points): The von Neumann Model

For this question, refer to the LC-3 version of the von Neumann Model below. The LC-3 is about to perform an instruction **FETCH**.

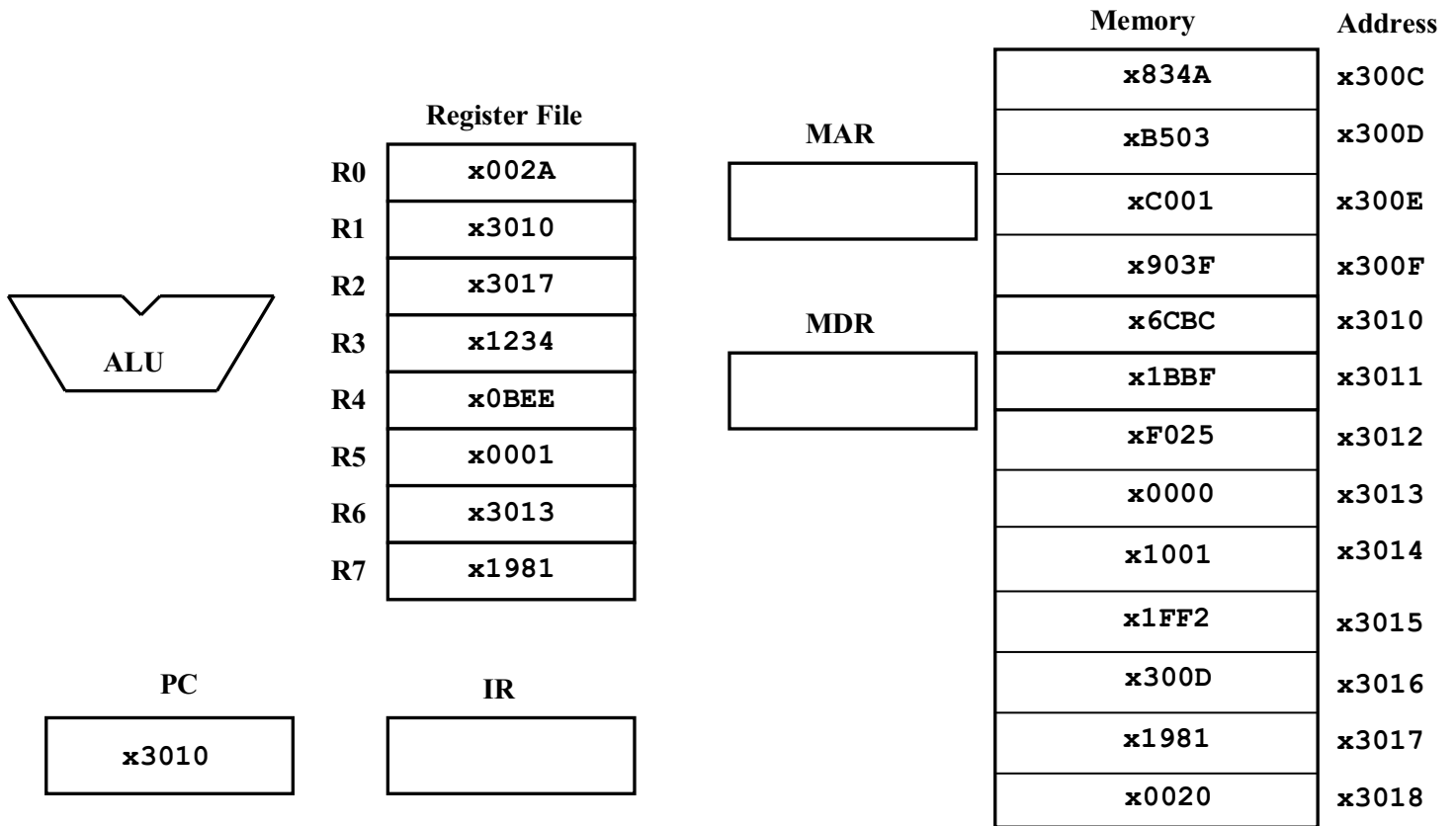
Say the LC-3 completes the execution of two instructions (i.e., the instruction cycle is performed twice). **Clearly indicate all final values in the diagram below for the...**

Part A (8 points): Register File

Part B (6 points): PC and IR

Part C (6 points): MAR and MDR

Hint: The instruction in **x3010** is an LDR instruction and the instruction in **x3011** is an ADD.



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Scratch Paper for Calculations

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD ⁺	0001			DR			SR1			0	00			SR2		
ADD ⁺	0001			DR			SR1			1	imm5					
AND ⁺	0101			DR			SR1			0	00			SR2		
AND ⁺	0101			DR			SR1			1	imm5					
BR	0000			n	z	p	PCoffset9									
JMP	1100			000			BaseR			000000						
JSR	0100			1	PCoffset11											
JSRR	0100			0	00			BaseR			000000					
LD ⁺	0010			DR			PCoffset9									
LDI ⁺	1010			DR			PCoffset9									
LDR ⁺	0110			DR			BaseR			offset6						
LEA ⁺	1110			DR			PCoffset9									
NOT ⁺	1001			DR			SR			111111						
RET	1100			000			111			000000						
RTI	1000			000000000000												
ST	0011			SR			PCoffset9									
STI	1011			SR			PCoffset9									
STR	0111			SR			BaseR			offset6						
TRAP	1111			0000			trapvect8									
reserved	1101															