

Instructions for Performing Experiments Involving VHDL in the Lab


Creating a Project

- Start Quartus II.
- From the *File* menu, select *New Project Wizard*.
- Enter a location, name, and top-level entity for the project. Create your project on the W: drive.
- Add any files that you have brought with you to the lab (you may need to copy them to the directory you specified above first).
- Select *Cyclone II* for Device Family
- Select *EP2C35F672C6* for Device
- Leave all other options at their default values and keep clicking *Next* until you get to *Finish*.
- You can see in the *Project Navigator* window at the left of the screen that a project has been created.


Adding Files to a Project

- If you didn't add your files in the step above, or if you wish to add additional files, right click on *Cyclone II: EP2C35F672C6* in the *Project Navigator* window on the left of the screen and click *Settings*. Select *Files* under *Category*. You can add files by entering their names directly or by finding them with the file browser; the *add all* button will add all vhd files in the project directory. Get the testbench files (*.vwf) from your TA and add to the project the same way as above. Additionally, in the *Settings* window, select *Simulator Settings* in the *Category* box, and set *Simulation Mode* to *Functional*, and set the given testbench file as the *simulation input*.

Analyzing, Synthesizing, and Implementing the Design



- Click the *Start Compilation* () button to begin the compilation process. If there are no errors, you will see each of the steps complete to 100%. If there are errors, you can view them on the *error* tab of the *Messages* window.
- You will need to fix any errors in your design before continuing. Additionally, you may receive warnings from the various steps. You should correct all warnings from the *Analysis & Synthesis* step. Warnings from the other steps may be acceptable; check with your TA.

Simulating the Design

- Once you are ready to run simulations on your design, select *Generate Functional Simulation Netlist* from the *Processing* menu. Once this process completes, click the *Start Simulation* () button. Verify that the simulation results are correct by selecting *View->Compare to Waveforms in File...* and selecting the same file you used for the input. The expected output values will be overlaid on the simulated output values; ideally, they should match, but it is possible to have a circuit that is functionally correct, just a few clock cycles off. Show the result to your TA.


Setting pin mappings and programming the DE2 Board

Once your design simulates correctly, you can download the design bit-stream onto the DE2 board and test it.

- First you have to provide pin assignments for inputs and outputs. Click the *Assignment Editor* button ()
- This will open the Assignment Editor. Select *Pin* in the dropdown menu. The list of pin assignments can be found in the lab manual entry for the current lab. Type in these assignments. (If you prefer, you can double-click the fields in the editor and select signals and pins from a dropdown menu.)
- Once you have entered the pin assignments for all ports, save the assignment editor view and recompile the design ()


Downloading the design to the DE2 Board

The Programmer sends the completed bitstream to the FPGA.

- Connect the programming cable to the computer's USB port and the board's *Blaster* connector.
- Power on the dev board.
- Click the *Programmer* button () to open the programmer. You should see a *.sof* file bearing the same name as the top-level entity in the window.
- If the box next to the *Hardware Setup...* button reads *No Hardware*, click the *Hardware Setup...* button and select the *USB-Blaster* option.
- Check the box under *Program/Configure* to select the programming file.
- Make sure the slider switch next to the LCD display on the DE2 board is set to *Run*, not *Prog*.
- Click *Start*. The FPGA will be programmed with your design.
- Once the programming process completes, test your design for functionality.
- If your design does not work or exhibits bugs, alter your design, recompile, and reprogram the FPGA. If you cannot easily determine how to fix your design, design a simulation to capture the incorrect behavior to better understand what is going wrong.

OPTIONAL - Programming the on-board PROM for power-on configuration

A PROM on the DE2 board will keep a copy of your FPGA design and program the FPGA after a board reset or power down. It is, however, not necessary for FPGA operation, and in fact takes quite a bit of time to complete; when debugging, this section can be ignored to save you time with each programming cycle.

- In the *Assignments* menu, click *Device*.
- Click the *Device & Pin Options* button.
- Go to the *Configuration* tab.
- In the dropdown menu next to *Use configuration device:*, select *EPCS16*.
- Click *OK* twice to close the *Device & Pin Options* and *Settings* windows.
- Recompile the design ()

- Open the programmer as before. In the *Mode* dropdown box, change *JTAG* to *Active Serial Programming*.
- A popup will appear asking if you wish to clear all devices. Click *Yes*.
- Click *Add File*.
- You should see a similarly-named file as before, but the extension reads *pof* instead of *sof*. Open this file.
- The *pof* file will appear in the window, with *Page_0* in an expansion beneath it. Click the *Program/Configure* checkbox next to the *pof* file. The box for *Page_0* will automatically become checked.
- Flip the slider switch next to the LCD display on the DE2 board from *Run* to *Prog*.
- Click *Start*.
- Once the process completes, turn off the DE2 board, flip the switch back to *Run*, and turn the board back on. The board should now be running with your design.

Design Statistics and Maximum Frequency

Note the design statistics (“Total Logic Elements” and “Total Registers”) and the maximum frequency from Compilation Report.

- Go to the *Compilation Report* tab (which opens automatically when you compile the design).
 - Analysis & Synthesis -> Summary (for Design Statistics).
 - Timing Analyzer -> Summary (for Maximum Frequency).