NON-EQUILIBRIUM

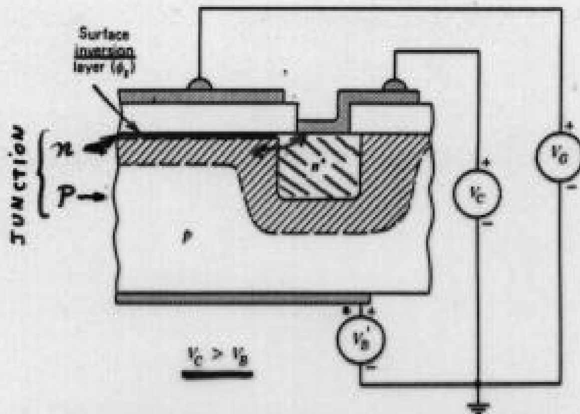


Figure 8.9 A diffused junction in the vicinity of an MOS capacitor can be used to bias the induced junction between the bulk of the silicon and an inversion layer formed at the oxide-silicon interface. The cross-hatching indicates the extent of the space-charge region in the depleted silicon.

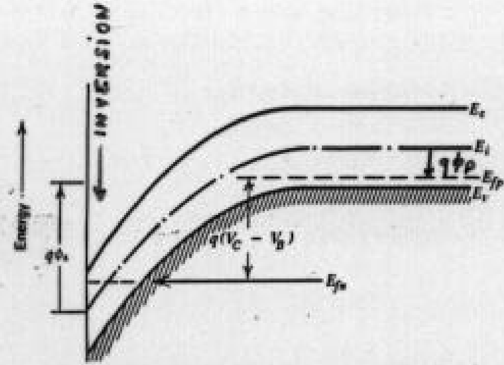


Figure 8.10 Energy-band diagram for an inverted surface on p-type silicon with a voltage $(V_C - V_B)$ applied between the inversion layer and the substrate.

SURFACE POTENTIAL FOR INVERSION

$$\phi_s = -\phi_p + (V_C - V_B) \qquad \phi_p < 0$$

↓ INCREASES Q_d (DEPLETION CHARGE)

↓ DECREASES n_s (INVERSION CHARGE)

$$x_{d\max} = \sqrt{\frac{2\epsilon_s(2|\phi_p| + V_C - V_B)}{qN_a}}$$

$$Q_d = -\sqrt{2\epsilon_s q N_a(2|\phi_p| + V_C - V_B)}$$

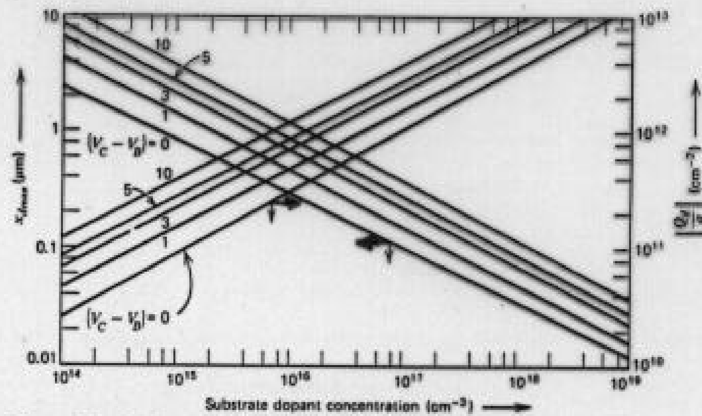
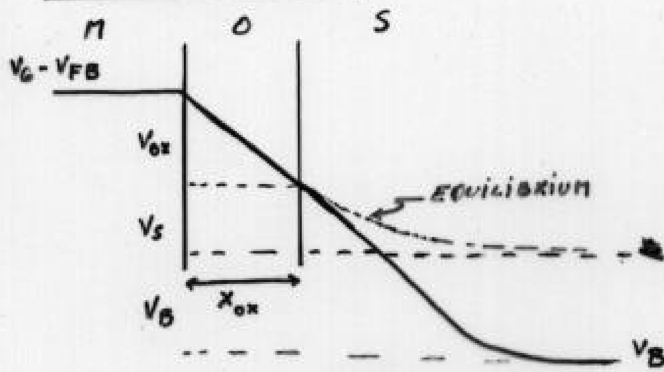


Figure 8.11 Maximum depletion-region width $x_{d\max}$ and corresponding area density of charges in the depletion region Q_d/q as functions of the substrate dopant concentration with the applied channel-to-substrate bias $(V_C - V_B)$ as a parameter. The curves are solutions to Equations 8.3.8 and 8.3.9.

THRESHOLD VOLTAGE



ONSET OF INVERSION

$$V_G - V_{FB} = V_{ox} + V_s + V_B$$

$$\begin{cases} V_S = \phi_S - \phi_p \\ \mathcal{E}_{ox} = \dfrac{V_{ox}}{X_{ox}} \end{cases}$$

$$= \frac{\epsilon_s}{\epsilon_{ox}} \mathcal{E}_s \qquad C_{ox} = \frac{\epsilon_{ox}}{X_{ox}}$$

$$\epsilon_s \mathcal{E}_s = C_{ox} [(V_G - V_B - V_{FB}) - (\phi_s - \phi_p)]$$

$$\boxed{-\epsilon_s \mathcal{E}_s = Q_s = Q_m + Q_d} \longleftarrow \boxed{\text{GAUSS}}$$

Q_m: FREE CHARGE; Q_d: DEPLETION CHARGE

$$Q_m = -C_{ox} [(V_G - V_B - V_{FB}) - (\phi_s - \phi_p)] - Q_d \qquad -Q_d = \sqrt{2\epsilon_s q N_a (2|\phi_p| + V_C - V_B)}$$

FROM $\phi_s = -\phi_p + V_C - V_B$

$$\boxed{Q_m = -C_{ox}(V_G - V_{FB} - V_C - 2|\phi_p|) + \sqrt{2\epsilon_s q N_a (2|\phi_p| + V_C - V_B)}}$$ PER UNIT AREA

V_T : THRESHOLD VOLTAGE : V_G $(Q_m = 0)$ ONSET OF INVERSION

$$\boxed{V_T = V_{FB} + V_C + 2|\phi_p| + \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_a (2|\phi_p| + V_C - V_B)}}$$

V_{FB}: FLAT BAND VOLTAGE; V_C: CHANNEL POTENTIAL; $2|\phi_p|$: SURFACE POTENTIAL; last term: DEPLETION

$$Q_m = -C_{ox}(V_G - V_T) \qquad \text{FOR } V_G \geq V_T$$

OXIDE AND INTERFACE CHARGE

ZERO BIAS | **FLAT BAND CONDITION**

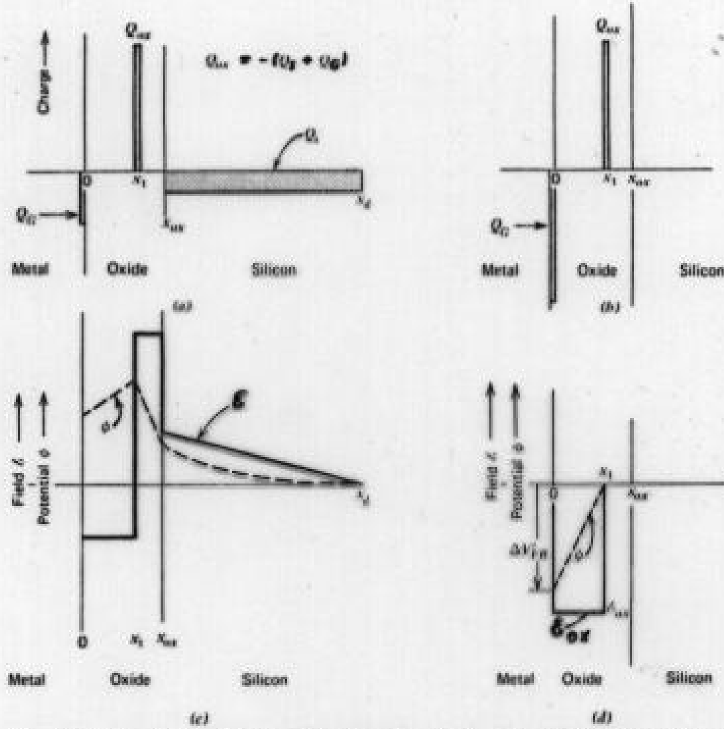


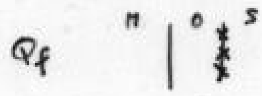
Figure 8.12 The effects of a fixed oxide-charge density Q_{ox} on the MOS system. (*a*) Charge configuration at zero bias: $Q_{ox} = Q_s + Q_G$; (*b*) charge at flat band: $Q_{ox} = Q_G$; (*c*) field (solid line) and potential (dashed line) at zero bias, (*d*) field (solid line) and potential (dashed line) at flat band. The silicon bulk is taken as the reference for potential in the diagrams for (*c*) and (*d*).

FLAT BAND VOLTAGE SHIFT

$$\Delta V_{FB} = x_1 \mathcal{E}_{ox} = -\frac{x_1 Q_{ox}}{\epsilon_{ox}} = -\frac{Q_{ox}}{C_{ox}}\frac{x_1}{X_{ox}}$$ ← FOR A δ-LIKE DISTRIBUTION

$$= -\frac{1}{C_{ox}}\int_0^{x_{ox}} \frac{x}{X_{ox}}\rho(x)\,dx$$ ← FOR A CONTINUOUS DISTRIBUTION

FIXED CHARGE AT THE $S_i - S_iO_2$ INTERFACE Q_f



$$\Delta V_{FB} = -\frac{Q_f}{C_{ox}}$$

GENERAL EXPRESSION OF THE FLAT BAND VOLTAGE

$$V_{FB} = \Phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{X_{ox}} \frac{x}{X_{ox}}\rho(x)\,dx$$

OXIDE AND INTERFACE CHARGE

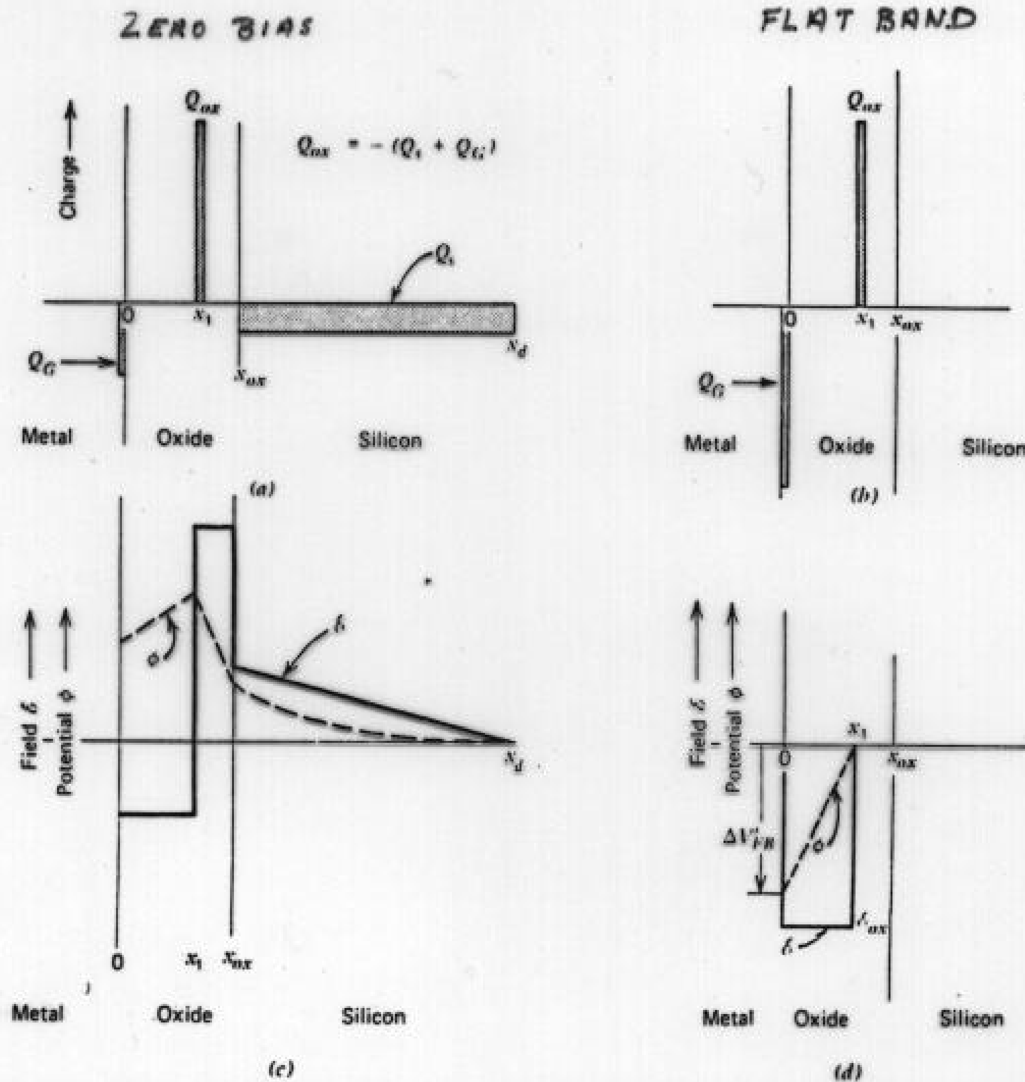


Figure 8.12 The effects of a fixed oxide-charge density Q_{ox} on the MOS system. (*a*) Charge configuration at zero bias: $Q_{ox} = Q_s + Q_G$; (*b*) charge at flat band: $Q_{ox} = Q_G$; (*c*) field (solid line) and potential (dashed line) at zero bias, (*d*) field (solid line) and potential (dashed line) at flat band. The silicon bulk is taken as the reference for potential in the diagrams for (*c*) and (*d*).

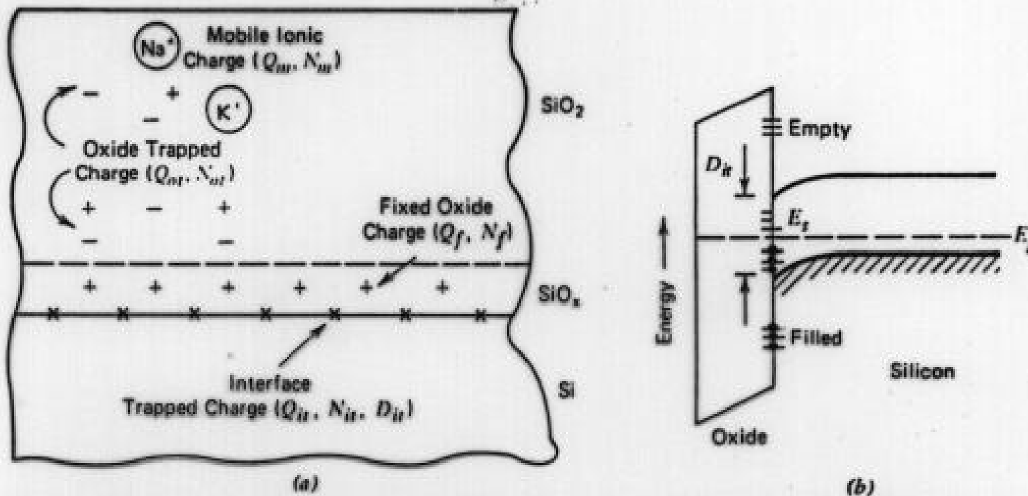


Figure 8.14 (*a*) Four categories of oxide charge in the MOS system. The symbols for the charge densities Q (C cm^{-2}), and state densities N (states cm^{-2}) or D (states cm^{-2} eV^{-1}) have been standardized.[4] (*b*) Energy levels at the oxide-silicon interface. The interface trapping levels are distributed with density D_{it} (states cm^{-2} eV^{-1}) within the forbidden-gap energies.

$Q_f > 0$ GENERALLY

$Q_{ot} > 0$ OR < 0 BUT GENERALLY SMALL

Q_m : MOBILE : INTRODUCED BY PROCESSING (HUMAN CONTACT)
→ INSTABILITIES IN V_T

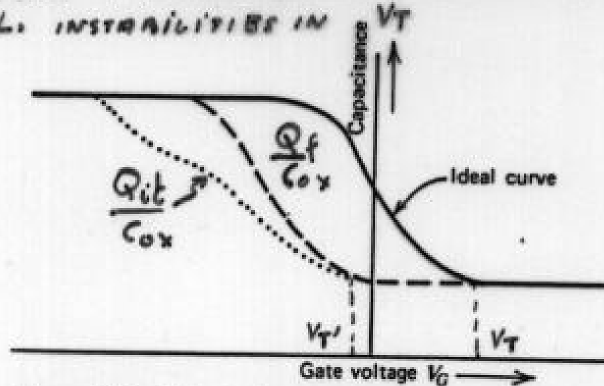


Figure 8.13 Fixed charge in the oxide causes the capacitance–voltage curve to translate along the V_G axis without distortion (dashed curve); charge that is influenced by the gate voltage causes distortion (dotted curve).

Table 8.2 Formulas for the Oxide-Silicon System

p-type substrate (*n*-channel)	*n*-type substrate (*p*-channel)
Flat-band voltage (*Equation 8.4.6*)	
$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x) dx$	
Bulk potential (*Equation* 4.2.9)	
$\phi_p = -\frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$	$\phi_n = \frac{kT}{q} \ln\left(\frac{N_d}{n_i}\right)$
Surface potential for strong inversion (*Table 3.1*)	
Thermal equilibrium $\phi_s = \lvert\phi_p\rvert$	$\phi_s = -\lvert\phi_n\rvert$
$\phi_s - \phi_p = 2\lvert\phi_p\rvert$	$\phi_s - \phi_n = -2\lvert\phi_n\rvert$
With bias $(V_C - V_B) = V_{CB}$	
$\phi_s = \lvert\phi_p\rvert + V_{CB}$	$\phi_s = -\lvert\phi_n\rvert - \lvert V_{CB}\rvert$
Maximum depletion width, x_{dmax} (*Equation 8.3.6*)	
Thermal equilibrium	
$\sqrt{\frac{4\epsilon_s\lvert\phi_p\rvert}{qN_a}}$	$\sqrt{\frac{4\epsilon_s\lvert\phi_n\rvert}{qN_d}}$
With bias V_{CB} (*Equation 8.3.8*)	
$\sqrt{\frac{2\epsilon_s(2\lvert\phi_p\rvert + V_{CB})}{qN_a}}$	$\sqrt{\frac{2\epsilon_s(2\lvert\phi_n\rvert + \lvert V_{CB}\rvert)}{qN_d}}$
Work-function difference, Φ_{MS}	
$\Phi_M - (X + E_g/2q + \lvert\phi_p\rvert)$	$\Phi_M - (X + E_g/2q - \lvert\phi_n\rvert)$
Threshold voltage V_T (arbitrary reference)	(*Equation 8.3.18*)
$V_{FB} + V_C + 2\lvert\phi_p\rvert + \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_a(2\lvert\phi_p\rvert + V_C - V_B)}$	$V_{FB} + V_C - 2\lvert\phi_n\rvert - \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_d(2\lvert\phi_n\rvert + V_B - V_C)}$