Chapter 2

Lab 2 - RF Oscillator

The goal of this lab is to design and construct a radio frequency oscillator. You will experiment with two different resonator variants: a quartz crystal and an LC tank that includes a voltage-controlled capacitor. You will also learn how to use the Vector Signal Analyzer for spectrum analysis. For useful examples and background information that pertains to this lab, you should read Chapter 5 (Oscillators) of the Class Notes.

2.1 Background Information

2.1.1 The Piezo Electric Quartz Crystal

Most oscillators employed for RF and microwave applications use a resonator to set the frequency of oscillation. It is desirable to use a resonator with the highest possible Q (lowest possible loss). Use of a high Q resonator generally guarantees that the phase of the loop gain will exhibit rapid variation near the frequency where it passes through 0. This means that the frequency of oscillation will be tightly constrained such that environmental changes that tend to alter the phase of the loop gain will not cause significant frequency shifts. In general, both the long-term and short-term stability of the oscillator is improved when the resonator has high Q. Resonators constructed using lumped inductors and capacitors typically have Q's on the order of 100 or so. This is sufficient for some applications, but a much higher Q can be obtained if a quartz crystal is used as an element of the feedback network.

To the circuit engineer the quartz crystal is a two-terminal passive network. The device is an electro-mechanical transducer which converts electric energy to mechanical energy and vice versa. The unit usually consists of a small quartz wafer sandwiched between two metal electrodes. In practice a quartz crystal will exhibit many resonance frequencies. It can be modeled electrically by the equivalent circuit shown in Figure 2.1 at frequencies near one set of resonance frequencies f_s and f_p.

The capacitance C_o is due to the parallel plate capacitor formed by the metal contacts that are used to hold the quartz wafer. The "components" r, L, and C in the equivalent circuit actually represent the effect of the mechanical vibration of the quartz wafer itself, and are referred to as the **motional components** of the model. Typical values for the equivalent circuit elements for a crystal with a fundamental resonance near 5 MHz are:

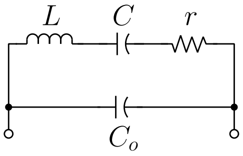

Figure 2.1: Quartz crystal circuit model

$$\begin{aligned} L &= 0.1\,\mathrm{H} \qquad (2.1)\\ C &= .01\,\mathrm{pF}\\ r &= 5\,\Omega\\ C_o &= 20\,\mathrm{pF} \end{aligned}$$

The reactance versus frequency characteristic for a crystal with these parameters will have the characteristic shape shown in Figure 2.2.

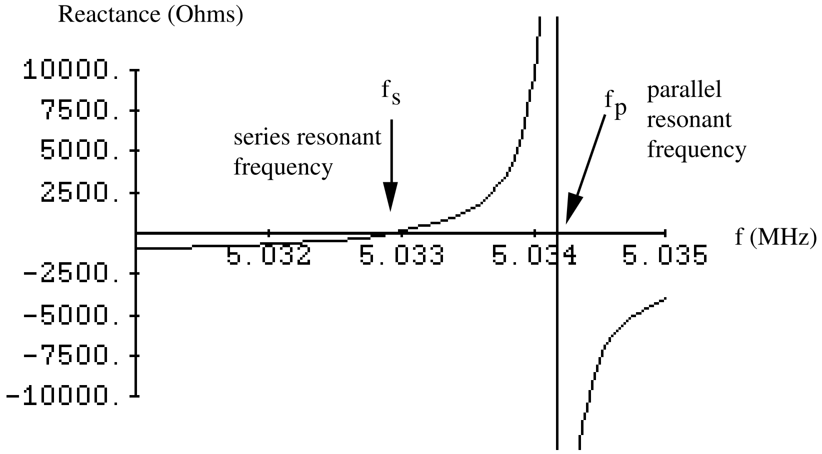

Figure 2.2: Crystal reactance versus frequency

This plot has been clipped and does not show the largest values of the reactance. Notice carefully that the frequency axis covers a range of only 4 kHz. The reactance curve exhibits a series resonance at f_s and a parallel resonance at f_p. The log of the real part of the crystal impedance is shown in Figure 2.3.

On a larger scale the resonance region on the reactance versus frequency plot would appear only as a small glitch on top of a capacitive reactance curve, e.g., if we plot reactance versus frequency at 50 points between 2 and 8 MHz, the curve would look like Figure 2.4.

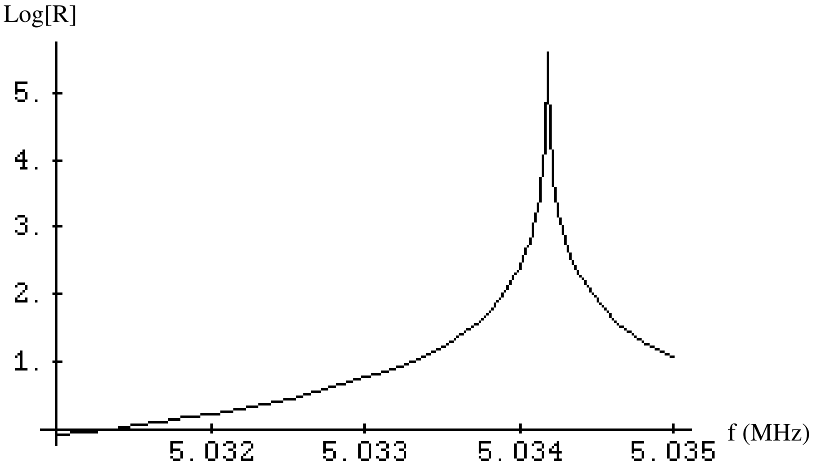

Figure 2.3: Logarithm of crystal resistance

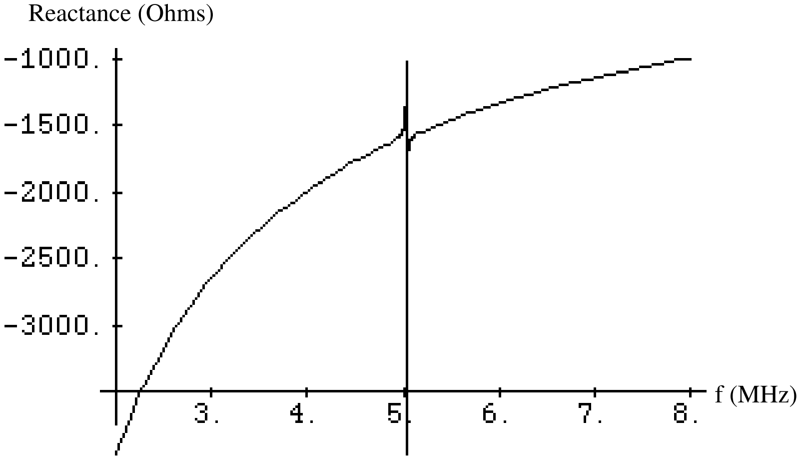

Figure 2.4: Expanded view of crystal reactance versus frequency

For a quartz crystal the parallel resonant frequency will be only a few hundredths of a percent larger than the series resonant frequency. Thus, the frequency range where the crystal looks inductive is very small - on the order of a few kHz for the crystals used in this lab. You should verify (by making use of the fact that $C \ll C_o$) that the ratio of the parallel and series resonant frequencies is well approximated by:

$$\frac{f_p}{f_s} \approx 1 + \frac{1}{2}\frac{C}{C_0} \tag{2.2}$$

In circuits a crystal is usually used to provide either a narrow-band "short circuit" or to act as an inductive reactance with very high Q. Circuit designers often refer to these possibilities as "series-mode" or "parallel mode" operation of a crystal, respectively. These are described below:

- Series resonant mode - the crystal is operated at f_s. Use is made of the fact that the crystal looks almost like a short-circuit at the series resonant frequency.
- Parallel resonant mode - operates between f_s and f_p where the crystal looks inductive. The circuit is designed so that the inductive reactance resonates with an external shunt capacitance. Here the crystal can be thought of as an extremely high Q inductor. Manufacturers will specify the external shunt capacitance required to make the crystal resonate at the frequency specified on the case. Typical values for the external load capacitance lie in the range 10-40 pF.

2.1.1.1 Measuring the Quartz Crystal

It is necessary to use care when using the VNA to measure the impedance of a component such as the Quartz Crystal. Near the resonant frequencies of the crystal the reactance changes very rapidly with frequency. In order to capture this behavior you will need to calibrate the VNA over a narrow range of frequencies centered on the resonant frequency of the XTAL. You will also need to use a slow sweep time so that the measurement dwell time is long compared to the duration of the transient response of the XTAL.

For your 10.245 MHz crystal, you should find that C_o is on the order of 5 pF. The value for the motional capacitance, C, should be very small - on the order of 0.01 pF. The value for L should be on the order of 10 mH. These values for L and C could not be realized using actual capacitors and inductors. For example, a 10 mH Henry inductor would consist of many (tens or hundreds) turns on a coil form, and such a coil would have a parallel resonant frequency well below the desired operating frequency. You should find that r is on the order of 10 Ω. The Q of a quartz crystal is defined in terms of the motional arm of the equivalent circuit, i.e., the series arm consisting of r, L, and C. By definition, the Q of a series resonant circuit is given by:

$$Q = \frac{\omega_s L}{r} = \frac{1}{\omega_s C r} \tag{2.3}$$

The Q of the crystal will typically be on the order of 50,000 or so.

2.1.2 Common Collector Oscillator Design

The heart of the oscillator consists of a single-transistor emitter-follower amplifier in a Colpitts configuration. In order to better understand the design of the oscillator circuit, its necessary to understand the small-signal mid-frequency model of a BJT transistor given in Appendix A of the Course Notes.

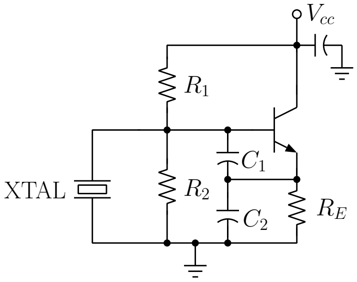

Figure 2.5: Common collector amplifier.

The gain for the oscillator will be provided by a common collector (CC) amplifier (also known as an emitter follower), as shown in Figure 2.5. As the first step in constructing this amplifier, you will need to calculate the appropriate values for the DC bias components R_1, R_2, and R_E. Unlabeled capacitors are bypass and coupling capacitors, respectively, and should have a very low impedance at the intended frequency of oscillation. In particular, a bypass capacitor (a capacitor used to connect a node to ground for AC signals) should have the lowest possible impedance at the operating frequency. A coupling capacitor (a capacitor used to couple one stage to another) need only have an impedance that is small compared to the load impedance that it couples to. Note that the bypass capacitor shown from V_{cc} to ground is important, as it is responsible for isolating the oscillator from the wires that connect the circuit to the power supply. Without this capacitor, the wires leading to the power supply and the power supply will all be a part of the circuit at the frequency of oscillation.

2.1.2.1 Design Base Bias Network

The oscillator will be powered by a +12 volt supply, and the output will be taken from the emitter. We will assume that the load impedance (denoted by R_L, not shown in Figure 2.5) is large compared to R_E, i.e. we assume $R_L \gg R_E$ so that the DC and AC load lines are approximately the same. In this case, a reasonable value for the quiescent base voltage is approximately $V_{cc}/2$:

$$V_{BQ} = 6\text{V}$$

The small signal gain of the transistor is proportional to the quiescent collector current, I_{CQ}. We will be eventually be using an inductor-varactor resonant circuit as the feedback element in the oscillator. Since this resonant circuit has a low Q, and hence high loss, we will need to have a fairly large loop gain to compensate. To achieve this, we choose

$$I_{CQ} \simeq 1 \text{ mA}$$

This value can be increased if the loop gain is found to be too small. Assuming that the base-emitter voltage drop across the transistor is 0.7 V, then $V_{EQ} \simeq 5.3$ V, so the required emitter resistance is $R_E \simeq 5.3\text{k}\Omega$. The closest standard value (e.g. $4.7\text{k}\Omega$) can be used.

Now, the bias network design can be finalized by determining values of R_1 and R_2 that will set the quiescent base voltage to the required 6V. There are two constraints to keep in mind. First, we desire the bias point to be insensitive to the precise value of transistor's short circuit current gain,

β. Second, we desire the parallel combination of $R_1||R_2$ to be as large as possible, because these elements appear in shunt with the resonator in a common-collector oscillator and will lower the Q of the resonator. Figure 2.6 presents the Thevenin equivalent circuit for the D.C. bias circuitry.

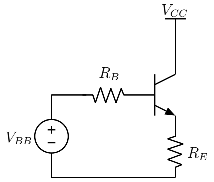

Figure 2.6: Thevenin equivalent circuit

The parameters V_{BB} and R_B can be calculated from:

$$V_{BB} = V_{CC}\frac{R_2}{R_1 + R_2}, \quad R_B = R_1 \parallel R_2 \tag{2.4}$$

The quiescent collector current can be calculated from this equivalent circuit:

$$I_{CQ} = \frac{\beta}{\beta+1}\frac{V_{BB} - V_{BEQ}}{R_B/(\beta+1) + R_E}. \tag{2.5}$$

To make I_{CQ} insensitive to temperature and device-to-device variation of V_{BEQ} and β the bias circuit should be designed so that I_{CQ}'s dependence on these quantities is minimized. This suggests that the following conditions should be satisfied:

$$V_{BB} \gg V_{BEQ} \tag{2.6}$$

$$R_E \gg \frac{R_B}{\beta+1} \tag{2.7}$$

The first condition guarantees that the quiescent current will be insensitive to variations in V_{BEQ} caused by temperature changes. If the base current is small, then $V_{BB} \simeq V_{BQ}$. We have already decided to make V_{BQ} approximately equal to $V_{cc}/2$, or 6 V; so the first condition will be satisfied. The second condition makes the bias point insensitive to variations in β. Data sheets for the 2N5179 transistor indicate that $25 \leq \beta \leq 250$. Thus, it is desirable to choose $R_B \ll 26R_E$. Since we have already determined that R_E should be near 5kΩ, this means that R_B should be small compared to 130kΩ. For example, if we choose R_B to be 50kΩ and R_E = 5kΩ then, with V_{BB} = 6V and V_{BEQ} = 0.7V, the bias network will hold the quiescent collector current to the range 0.74 mA $\leq I_{CQ} \leq$ 1.02 mA. Smaller values of R_B will make the collector current even less dependent on β, but we should remember that R_B appears in shunt with the resonator in the common-collector Colpitts configuration, and smaller values of R_B will result in smaller Q for the tank.

To get a feeling for the tradeoff involved in choosing R_B we can look ahead to the final configuration of the oscillator where we will be using an LC resonator to cause the circuit to oscillate near 100 MHz. The net capacitance will be the parallel combination of a varactor diode and the series combination of C_1 and C_2. Let us assume that the net capacitance will be on the order of 100 pF. Then, the inductance will be L = 250 nH. At 100 MHz, the impedance of the inductor will be about $j150\ \Omega$. The largest Q that we could expect the inductor to have is on the order of a few hundred. Say $Q_L = 250$. Then the equivalent parallel resistance of the inductor is $250(150) = 37.5\ \mathrm{k}\Omega$. Since R_B appears across the inductor, if $R_B = 50\ \mathrm{k}\Omega$, the net parallel resistance will be $37\ \mathrm{k}\Omega || 50\ \mathrm{k}\Omega = 21\ \mathrm{k}\Omega$. Assuming that the resonator Q is entirely determined by this resistance, then we can say that adding R_B in parallel with the resonator would reduce the resonator Q from 250 to $\frac{21}{37.5}250 \simeq 140$. Smaller values of R_B would improve bias stability at the expense of more serious degradation of the resonator Q.

In its final configuration, the oscillator will use a varactor/inductor resonator, and the varactor has relatively low Q. In fact, the MV104 tuning diode that we will use is specified to have a typical Q of 140 at 100 MHz. Hence the inductor/varactor combination will undoubtedly have resonant Q_p smaller than 100 at 100 MHz. In this case, even smaller values of R_B can be used without significantly compromising the tank circuit Q. You should now have enough information to determine the values of R_1 and R_2 in your circuit. It is suggested that you assume that the intrinsic Q_p of the resonator will be on the order of 100, and that you choose R_B to degrade this value to a value no smaller than 80.

2.1.2.2 Choose C_1 and C_2

Now that we have determined how to bias the transistor at a suitable quiescent point, we must turn our attention to the small signal amplification. The common collector is a current amplifier with a voltage gain close to unity. As discussed in the course notes, the base-emitter voltage swing is controlled by the ratio C_1/C_2. It is desirable to keep the base-emitter voltage swing relatively small, which results in the most sinusoidal output voltage. To achieve this, choose C_1 and C_2 such that

$$C_1/C_2 \gg 1$$

Additionally, we would like to choose C_1 to be much greater than the input capacitance of the transistor (˜10pF). This will tend to make circuit performance relatively independent of the junction capacitance of the transistor, and mainly dependent on the values of external circuit elements which are under our control. The first oscillator circuit that we will build uses a Quartz crystal in parallel resonance with the series combination of C_1 and C_2. In our circuit, the crystal resonates with the series combination of C_1 and C_2 (where C_1 should include the base-emitter capacitance of the transistor, which is approximately 10 pF). Earlier, you determined what this load capacitance should be in order for the circuit to oscillate at the desired frequency (10.245 MHz). Hence we should choose values of C_1 and C_2 that provide the desired load capacitance for the Quartz crystal. You should now have enough information to determine initial values of C_1 and C_2.

2.1.3 Active Buffer Design

In order to drive a low-impedance load such as 50 Ω, we need to add an impedance matching device that converts the low impedance load to a high impedance that the oscillator can drive. We could use a simple L-net to transform the load impedance, but this would only work for one frequency and we will later use be using a varactor to tune the frequency of oscillation. For this reason, we will use another CC amplifier, acting as a broad-bandwidth active impedance match or buffer. As you may recall, a CC amplifier has high input impedance and relatively low output impedance. Thus, we can drive a 50 Ω load with the addition of this buffer stage, as shown in Figure 2.7.

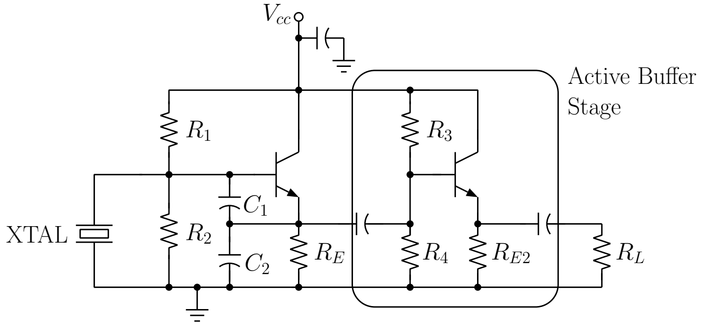

Figure 2.7: XTAL oscillator with active buffer.

2.1.3.1 Biasing the emitter follower buffer stage

Consider the DC and AC load lines for an emitter follower, as shown in Figure 2.8.[1] The emitter voltage is plotted against the collector current, I_C, which is assumed to be approximately equal to the emitter current. When the circuit is excited with a time-varying input signal, or when the circuit is oscillating, the instantaneous emitter voltage and current will be related by the AC load line.

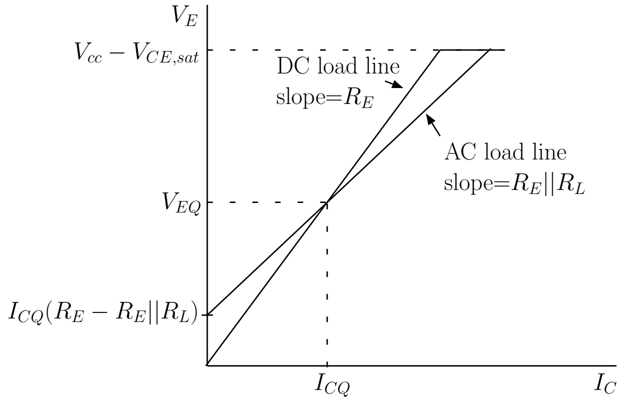

Figure 2.8: DC and AC load lines for the emitter follower amplifier.

Notice that the instantaneous emitter voltage can swing between a minimum value $V_{E,min} = I_{CQ}(R_E - R_E||R_L)$ and a maximum value $V_{E,max} = V_{CC} - V_{CE,sat}$. Typically, the collector-emitter saturation voltage is taken to be $V_{CE,sat} \simeq 0.1$ V so that $V_{E,max} = V_{CC} - 0.1$ V. At the upper limit, the emitter voltage is limited at $V_{CC} - 0.1$ V due to transistor saturation. At the lower limit, $V_{E,min}$ corresponds to transistor cutoff, since the corresponding instantaneous collector

---

[1] We will use the symbol R_E to refer to the emitter resistance in a generic emitter-follower amplifier. This corresponds to R_{E2} in Figure 2.7.

current is zero. For the minimum and maximum emitter voltage swings to be symmetrical around the quiescent point, we require

$$V_{CC} - 0.1 - V_{EQ} = V_{EQ} - I_{CQ}(R_E - R_E||R_L)$$

Using $I_{CQ} \simeq V_{EQ}/R_E$ and solving for V_{EQ} yields an expression for the quiescent emitter voltage under conditions of maximum symmetrical emitter voltage swing:

$$V_{EQ,ss} = (V_{cc} - 0.1)\frac{R_E + R_L}{R_E + 2R_L}.$$

When the transistor is biased at this quiescent point, the maximum undistorted zero-to-peak voltage swing across the load will be

$$V_{0-p,ss} = (V_{cc} - 0.1)\frac{R_L}{R_E + 2R_L}.$$

If V_{EQ} is less than $V_{EQ,ss}$ then the output voltage swing will be limited on negative excursions by transistor cutoff. In this case, the maximum undistorted 0-peak swing will be

$$V_{o-p} = V_{EQ}\frac{R_L}{R_E + R_L}.$$

If V_{EQ} is greater than $V_{EQ,ss}$ then the output voltage swing will be limited on positive excursions by transistor saturation. In this case, the maximum undistorted 0-peak swing will be

$$V_{o-p} = V_{cc} - 0.1 - V_{EQ}.$$

The power dissipation limits of the transistor and the emitter resistor must be considered as well. The DC power dissipated in the transistor is $\simeq (V_{CC} - V_{EQ})I_{EQ}$. The power dissipated in the emitter resistor will be the sum of the DC power $(V_{EQ}I_{EQ})$ and the AC power, which depends on the drive level.

To save you some time, we will tell you that your best bet is to choose an emitter resistor $R_E \simeq 300\ \Omega$ and a quiescent emitter current $I_{EQ} \simeq 20$ mA. This means that $V_{EQ} \simeq 6$ V. With these values, and assuming $V_{cc} = 12$ V, the value of $V_{EQ,ss} = 10.4$ V. Since $V_{EQ} < V_{EQ,ss}$, the output voltage swing will be limited on negative excursions by transistor cutoff. The maximum undistorted 0-peak emitter voltage swing will be 0.86 V. This is also the 0-peak voltage across the load, so the maximum output power without significant waveform distortion will be $0.86^2/(2*50) = 7.4$ mW, adequate to drive the mixer.

With $V_{EQ} = 6$ V, the DC power dissipated in the transistor will be approximately $5.9\ \text{V} * 0.02\ \text{A} = 118$ mW, which is within the maximum dissipation limit (200 mW) of a 2N5179 transistor. The DC power dissipated in the emitter resistor will be approximately $6\ \text{V} \times 0.02\ \text{A} = 120$ mW, also within the dissipation limits of a 1/4 Watt resistor. If you decide to choose a different quiescent point, be sure to check the power dissipated in the transistor and in the emitter resistor. You may obtain larger output voltage swing, and smaller power dissipated in the transistor by raising V_{EQ}. On the other hand, power dissipated in the emitter resistor will increase if V_{EQ} is raised, in which case it may become necessary to use something larger than a 1/4 Watt resistor for R_E.

Choose value for R_3 and R_4 that set the bias point to the desired value. Note that $R_B = R_3||R_4$ will have to be significantly smaller here than it was for the oscillator stage. With $R_E = 300\ \Omega$ and $\beta_{min} = 25$, we need to keep R_B much smaller than 7.8 kΩ.

To avoid significant output waveform distortion you will need to make sure that the buffer amplifier is not overdriven by the oscillator. If your oscillator output is too high, two ways to decrease the drive level to the buffer amp are (i) decrease the loop gain of the oscillator to decrease the steady-state oscillation amplitude. This can be done by inserting a resistance in series with the $C_1 - C_2$ junction and the emitter of the transistor; or (ii) use an attenuator in between the oscillator and the emitter follower. A simple resistive L network (voltage divider network) will suffice. Design the network so that the impedance presented to the oscillator is high and the impedance presented to the emitter follower is (relatively) low. This means that the series arm of the resistive L-net connects to the oscillator, and the shunt arm connects to the emitter follower.

2.2 Voltage Controlled Oscillator Design

Now, we're ready to construct a Voltage Controlled Oscillator (VCO). Our VCO will be constructed by replacing the capacitor tank capacitor with a varactor diode, as shown in Figure 2.9.

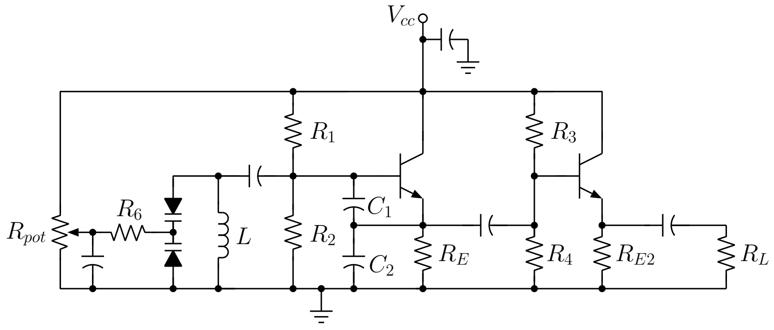

Figure 2.9: Voltage-controlled oscillator with tuning potentiometer.

2.2.1 Varactor

The varactor is a variable capacitor derived from the junction capacitance of a reverse-biased diode. As the tuning voltage increases, the varactor is increasingly reverse-biased, leading to a larger depletion region and thus a smaller capacitance. This gives us control over the frequency of oscillation. Notice that, in our design, we use two varactor diodes back-to-back, to simplify biasing. The two back-to-back varactors help to ensure that neither varactor diode is driven into forward bias. With the dual-diode scheme, half the tank voltage appears across each diode. If the voltage swing is large enough to drive a diode into conduction, the other diode will be strongly reverse biased. So the impedance across the tank will always be high. If only a single diode was used, then when the diode is driven into conduction, the low diode impedance would appear across the tank circuit, and will quickly drain the energy from the tank, dramatically reducing the effective Q of the tank.

2.3 Lab 2 Step-by-Step Guide

2.3.1 Equivalent Circuit of a Quartz Crystal and Parallel Resonance:

1. Using the technique and setup from Lab 1, measure the reflection from your quartz crystal (don't forget to trim leads to 1 cm). Set *start* and *stop frequencies* to 7 and 11 MHz respectively. Calibrate the instrument and take the measurement, saving thedata as in Lab 1. Measure the reactance on the lower end of the measured frequencies(at least 1% lower than the frequency marked on the case)and **determine the package capacitance** C_o using :

$$C_o \simeq -\frac{1}{2\pi f X} \tag{2.8}$$

2. Repeat the calibration and measurent for a narrow frequency range (e.g. 10.23 to 10.27 MHz, 6401 pts; also set [Sweep][IF Bandwidth] to 500 Hz and set [Sweep][Sweep Time] to 50 sec.) to focus on the resonant region. **Measure and record** f_s **and** f_p, the series and parallel resonant frequencies of the crystal. The crystal impedance will be smallest at the series resonant frequency of the motional arm, f_s. At the series resonant frequency of the motional arm, f_s, the crystal impedance will be approximately equal to the motional resistance, r. **Record the value of** r. You can use the marker on the Smith chart display format in VNA, and later verify the value in ADS.

3. **Determine** C using the equation 2.2.

4. **Determine** L using the values for C and f_s. L and C are series resonant at f_s, so that

$$L = \frac{1}{(2\pi f_s)^2 C} \tag{2.9}$$

5. **Compute the** Q of your crystal using equation 2.3

6. From the reactance plot between the two resonant frequencies, determine the reactance of the crystal at 10.245 MHz, the desired frequency of oscillation. **Calculate** C_L, the load capacitance that will resonate with the crystal at this frequency.

7. Measure parallel mode resonant frequencies of the crystal placed in the fixture in parallel with several capacitors provided by your TA. Record the resonant frequencies, calculate capacitance values for the mystery capacitors. You can use equation 2.2 since the capacitors appear in parallel (added) with C_o.

2.3.2 Construction of the Oscillator with Xtal Feedback:

8. Describe the role and determination of appropriate values for the biasing resistors R1, R2, and Re.

9. Prepare the PCB subassemblies to soldering by lightly sanding the surfaces

10. Short the via holes with wire wrapping wire soldered to tob and bottom. Make sure not to obstruct component pads.

11. Solder the transistor to the PCB pads. Visually examine the quality of contacts.

12. Solder the biasing resistors, the RC for the voltage supply, and the coupling capacitors.

13. Solder a convenient way to connect voltage supply output to the Vcc pad. Connect the DC power, ramp up to 12 V.
14. Measure and record DC bias voltages at each pin of the transistor. Note the current draw at the power supply.
15. (Disconnect from voltage source before soldering every time.) Solder C1 and C2. Re-measure DC bias voltages at each pin of the transistor.
16. Solder the crystal, completing the oscillator circuit. Once again, measure DC bias voltages.
17. Verify that the circuit is oscillating by looking at the output on an oscilloscope. Use a x10 scope probe to monitor the waveform at the emitter of the transistor. Measure the peak-to-peak voltage and comment on some of the characteristics of the waveform, i.e. distortion. What is causing this distortion? Is the transistor being driven to cutoff or saturation? Connect the scope probe to a frequency counter and record the oscillation frequency.
18. Measure oscillator output on the oscilloscope for 1 MΩ and 50 Ω scope input impedance, with and without a 10x probe. Save the traces via a diskette. Compare the four cases.
19. Measure oscillator frequency of oscillation on the oscilloscope. Use frequency counter to measure the more precise frequency value.
20. Observe the changes to the output waveform after making the circuit changes described by your TA. Measure and save scope traces.
21. Comment on your measurements and observations.

2.3.3 Construction of the Xtal Oscillator with Buffer Amp:

22. Construct the buffer amplifier with suggested initial values: $R_3 = 1.2k\Omega$, $R_4 = 1.5k\Omega$, $R_{e2} = 300\Omega$
23. Connect the SMA cable from the output to the 50Ω input of the oscilloscope. Check if the circuit is oscillating. If so, save the scope trace.
24. If the circuit is not oscillating, increase the transconductance (and oscillator gain) by decreasing R_e of the oscillator (suggested: $3k\Omega$). Check if the circuit is oscillating. If so, save the scope trace.
25. If the circuit is not oscillating, increase the loop gain by increasing C_2 of the oscillator (suggested: $30pF$). Check if the circuit is oscillating. If so, save the scope trace.
26. If the oscillations show significant distortion (i.e. clipping), increase the bias voltage of the buffer by increasing R_4 (suggested: $2.4k\Omega$). Save the scope trace.
27. (Optional) To reduce distortions further, add a series load (suggested: 300Ω). Save the scope trace.
28. Connect the output to VSA. Adjust the instrument settings to display the 10.x MHz peak and six more harmonics. Record the powers of the fundamental and several more strong harmonics. (Hint: use marker functions). Save the VSA plot.
29. Adjust VSA settings to zoom in on the fundamental frequency. Using the procedure attached at the end of the lab 2 instructions, measure frequency drift and the effect of hand capacitance on frequency.

30. Measure the phase noise of the oscillator using the attached procedure. Note the settings required. Record the value at a given frequency offset. Save the plot.

2.3.4 Construction of the VCO:

31. Remove the crystal from the board
32. Attach the SMD inductor (56 nH) and the varactor (SOT23 package, like transistor)
33. Attach the bypass RC combination and the varactor
34. Check if you see any oscillations on the oscilloscope (SMA, 50Ω connection). Likely, you will not see any.
35. If you have a loading resistor connecting the oscillator to the buffer, remove it and replace by coupling capacitor.
36. Replace C_1 with 33 pF. Check for oscillations on the scope. If oscillating, turn the potentiometer to check the tuning range.
37. Replace C_2 with 3.3 pF. Check for oscillations on the scope. If oscillating, turn the potentiometer to check the tuning range. If you have less than 1.5 Vpp oscillation, check with TA for advice.
38. Once you have made sure that power and frequency range are within spec, move on to characterization.
39. Make a table with the following columns: frequency, power, V_{var}, C_{total}, C_{var}. Use marker and peak tracking on VSA. Set frequency span to include the whole tuning range. Cover the tuning range in 5 MHz steps while filling the table frequency, power, and voltage (use multimeter) columns. Calculate the capacitance columns. Plot P vs. f, and C_{var} vs. V_{var}.
40. Adjust VSA settings to zoom in on the fundamental frequency tuned to the middle of the required range. Using the procedure attached at the end of the lab 2 instructions, measure frequency drift and the effect of hand capacitance on frequency.
41. Measure the phase noise of the oscillator using the attached procedure. Note the settings required. Record the value at a given frequency offset. Save the plot.

2.4 Lab 2 Procedures

2.4.1 Spectrum Analysis with the Agilent 89441A Vector Signal Analyzer

The Agilent 89441A Vector Signal Analyzer is comprised of two modules. The back end, or IF section (the box on top), consists of a 10 MHz lowpass filter (anti-aliasing filter) followed by a high speed analog to digital converter and a Digital Signal Processor (DSP). This unit is capable of performing a wide variety of signal processing functions on any signal contained within the frequency range 0-10 MHz. The front end, or RF Section (the box on the bottom), consists of multiple filters and mixer/LO stages comprising a triple-conversion superheterodyne mixing scheme which can convert a 7 MHz wide slice of the RF spectrum centered on any frequency in the range 2 MHz -

2.65 GHz to the 0-10 MHz range that can be processed by the back end. The triple conversion scheme employed by the 89441A's front end uses IF's of 3046 MHz, 46 MHz, and 6 MHz to process a slice of the spectrum with a bandwidth of 7 MHz.

The ability of a spectrum analyzer to resolve two closely-spaced spectral lines is determined by the "Resolution Bandwidth" (RBW) of the instrument. The IEEE definition of spectrum analyzer Resolution Bandwidth is: " . . . the ability to display adjacent responses discretely. The measure of resolution is the frequency separation of two responses which merge with a 3 dB notch." The Agilent 89441A VSA captures a signal of interest in the time domain and calculates the spectrum using a fast Fourier transform (FFT). The RBW of the 89441A will be determined by the length of the data sequence that is captured and by the shape of the window function that is used to taper the data window before performing the FFT. For a given window function the RBW will be inversely proportional to the length of the data sequence. Thus, small RBW's require long time series.

2.4.1.1 Laboratory Exercises

The following exercises are intended to help you become familiar with the spectrum analysis capabilities of the 89441A VSA. You are also encouraged to utilize the 89441A's online help system which can be accessed by pressing the [**Help**] button.

Note: When turning on the Vector Signal Analyzer always turn on the RF Section (the bottom box) first, and then turn on the front end (the top box, with display.

Section I - Basic Operation of the VSA for spectrum analysis

1. Press the green **PRESET** button. This will set the VSA to its initial state.
2. Select the RF section as the input:
   [**Instrument Mode**][receiver][RF(2-2650MHz) normal]
3. Connect an external signal generator to the INPUT port on the 89441A RF section. Set the signal generator to output an unmodulated carrier at frequency 250 MHz. Set the output power of the signal generator to -10 dBm.
4. Set the Frequency span.
   [**Frequency**][center] 250 MHz [span] 1 MHz
   On the display, you should see the "spike" associated with the signal at 250 MHz.
5. Set a marker on the peak of the spike:
   [**Marker ->**][marker to peak]
   How does the signal power measured by the VSA compare to what you expected?
6. Experiment with changing the resolution bandwidth (RBW) of the VSA.
   [**ResBW/Window**] and use the ↑ and ↓ arrow keys to change the RBW. As the RBW is decreased the instrument must use a longer time series to calculate the spectrum and hence the time to update the display will increase. Note carefully that as the RBW is increased, the width of the displayed spike becomes wider. The shape the spike has nothing to do with the spectrum of the signal from the signal generator (which is actually nearly a "delta function"). The shape of the spike reflects the Fourier transform of the window function that was used to taper the time-series data. Use the markers to make a careful measurement of the -3 dB bandwidth of the displayed "spike". Compare this value with the RBW.

7. Turn video averaging on in order to make an accurate measurement of the noise floor.
   [**Average**][average on]
   This function averages the data before displaying it on the video monitor. The default number of points averaged is 10. With averaging on, move the marker to the noise floor and note what happens to the noise floor as the RBW is increased or decreased. Record your observations.

8. In its default state, the VSA is not able to detect very weak signals. The sensitivity is controlled by the setting of the Range parameter. Change the setting of the external signal generator to decrease the available output power to -110 dBm. Notice that the signal is no longer detectable on the VSA display. Now increase the sensitivity of the VSA as follows:
   [**Range**] and use the ↓ button to decrease the range to the minimum value (-50 dBm). Notice that the very weak signal from the signal generator is now detectable. In this state the VSA is an extremely sensitive receiver - but it is very susceptible to overload from strong signals. The range setting is the maximum input power level that can be tolerated by the instrument - so any signal that is larger than -50 dBm will cause the "OV1" error message to display. *If strong signals overload the input of the VSA, spurious signals will be generated within the VSA and the displayed spectrum will not reflect the true input spectrum.*

Section II - The Spectrum of a Television Station

1. Connect an outside antenna to the VSA. (Consult your TA.) Channel 3 (WCIA) is located between 60 and 66 MHz. Change the VSA so WCIA occupies the entire display.
2. Turn on Video Averaging.
3. Obtain a plot of the spectrum. Label the carrier, color subcarrier and sound carrier.

Determination of the Horizontal Sweep Frequency

You have just looked at the spectrum using a large RBW. More information about the television signal can be obtained if you zoom in on each of the components. The television signal spectrum has an interesting "fine structure" due to the quasi periodic nature of the horizontal and vertical scan and the associated "sync" pulses.

1. Center the carrier. Try [**Marker ->**][peak], [**Marker ->**][center frequency]. Narrow the span to 100kHz. Adjust the RBW so that the frequency components due to the horizontal scan and sync can be easily identified. You may wish to turn video averaging on to obtain a smoother display.
2. Measure the Δ in frequency between the impulses. Reconcile the measured horizontal sweep frequency with the expected horizontal sweep frequency. Obtain a plot.

Determination of the Vertical Sweep Frequency

The television signal also has frequency components due to the vertical sync.

1. Center one of the horizontal spectral components. Change the span to: 200-500Hz.
2. Adjust the VSA so that the frequency components due to the vertical sync can be easily identified.
3. Measure the Δ in frequency between the impulses. Reconcile the measured vertical sweep frequency with the expected vertical sweep frequency. Obtain a plot.

Color Subcarrier

Zoom in on the subcarrier. Find the frequency components due to both the horizontal and the vertical sync. Obtain a plot.

Sound Carrier

Zoom in on the sound carrier. Use video averaging and estimate the BW of the FM signal at the -20 dB points. Obtain a plot.

2.4.1.2 Measurements for Oscillator Characterization

- Measure the output power (in dBm) and frequency of the fundamental harmonic. Compare this to what you observed on the oscilloscope.
- Record the frequencies and output powers of the first seven harmonics. Estimate the total harmonic distortion (THD) from the output spectrum. Use the first five harmonics to estimate THD. THD (in percent) can be calculated as follows:

$$THD \text{ (percent)} = \frac{\text{total power of all harmonics above fundamental}}{\text{total output power of signal}} \times 100$$

- How stable is the output at the fundamental frequency (i.e. is there any frequency drift over time)? Quantify this drift by setting up the delta marker:
  - Marker Func | Peak Track ON | Frequency Counter ON
  - Marker | Offset Marker ON | Zero Offset
  - Use a span of 100 kHz and RBW of 300 Hz. Observe for one minute and record the largest frequency drift. How susceptible is the output frequency to stray capacitance (e.g. hand capacitance)?
- Measure the phase-noise spectral density of the oscillator at an offset of 1 kHz from the carrier. Use the following procedure to set up the VSA to perform a phase demodulation and spectral analysis of the resulting demodulated phase waveform:
  - [Marker to Peak][Marker → Center]
  - Span = 20 kHz, RBW = 1 kHz
  - [Inst Mode] → [Demodulation]
  - [Demod Type] → [Analog] → [Return]
  - [Demod Setup] → [Ch1 Result] → [PM]
  - [Average ON]
  - Print out graph of phase variance vs. frequency offset.· Measure the phase variance at a 1kHz offset. For the XTAL oscillator, you may notice that the phase variance at a 1kHz offset is in the noise floor. To accurately measure phase variance for the XTAL oscillator, set your span to 1kHz and your RBW to 10Hz. This will show a zoomed-in picture of the phase variance for a frequency offset of 0 to 500Hz. Print out this graph if necessary.