ECE 482
Course Information

Fall Semester 2009 Professor E. Rosenbaum

Class Meetings
3 PM – 3:50 PM, 241 Everitt Lab

Instructor
Professor Elyse Rosenbaum
Office Hours: Wednesday 9:00 AM – 10:00 AM, 407 CSL
Thursday 2:00 PM – 3:00 PM, 407 CSL
Email: elyse@illinois.edu

Teaching Assistant
Hongbo Zhang
Office Hours: Monday 9:30 AM – 10:30 AM, 330N EL
Friday 4:00 PM – 5:00 PM, 330N EL
Email: zhanghongbo1209@gmail.com

Textbook
J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, *Second Edition*, Prentice Hall, 2003.

Other Reference Books (on reserve at Grainger Engineering Library)
A. Vladimirescu, *The Spice Book*, John Wiley & Sons, 1994.
D. Hodges, H. Jackson and R. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology, Third Edition*, McGraw-Hill, 2004.
S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits, Third Edition*, McGraw-Hill, 2003.
K. Bernstein *et al., High Speed CMOS Design Styles*, Kluwer, 1998.

Grading
Weekly Homework 15%
Homework is due in class on the due date, preferably before the lecture begins. If you arrive late to class, do not disrupt the lecture by walking to the front of the room to hand in your homework; instead, give it to the instructor or the TA immediately after the lecture is concluded. If you will not be able to attend class due to a job interview, conference trip, etc., you may turn in your homework early to the T.A. or the instructor. Late homework will not be accepted, except under unusual circumstances at the instructor's discretion. We will drop each student's lowest homework grade of the semester before calculating the semester totals; therefore, students who fall ill during the semester should not request a make-up assignment. A student who is seriously ill for more than 7 consecutive days should contact the instructor. Homework solutions will be posted on the class web page. Homework is to be the student's own work, not a collaborative or plagiarized work. However, students are permitted and encouraged to help one another by engaging in discussion of course material and approaches to solving the homework problems.
First Midterm Exam 15%
Second Midterm Exam 15%
Final Exam 30%
Design Project Report 25%
Students will work in instructor-assigned groups of four. Reports will be due in class on Dec. 9. All the members of a group will receive the same grade except in the case that a group member does not make a good faith effort to contribute significantly. The design project assignment will be provided on or around Oct. 28.

ECE482 Web Page
http://courses.ece.illinois.edu/ece482/
Check the web page a few times per week; this is where corrections to homework assignments and changes to office hours will be posted. Tutorial material will also available on our web page. A web-based forum has been set up:

http://my.ece.uiuc.edu/webboard/board.asp . All questions regarding the homework assignments or solutions should be posted to the web-board. It is the **primary** means of staff-student communication outside of class hours. The TA or instructor will check this forum often and will post responses to any queries.

ECE 482 Syllabus (*Tentative, subject to modification)*

Fall Semester 2009 Professor E. Rosenbaum

1. 8/24 Introduction & terminology
2. 8/26 MOSFET threshold voltage
3. 8/28 MOSFET I-V model
4. 8/31 Static characteristics of inverter
5. 9/2 Previous topic, cont'd
6. 9/4 Dynamic characteristics of inverter
7. 9/9 Device and interconnect capacitance
8. 9/11 Power
9. 9/14 Layout and circuit simulation tools
10. 9/16 Inverter sizing and delay
11. 9/18 Inverter chain
12. 9/21 Combinational logic: Complementary static CMOS
13. 9/23 Previous topic, cont'd
14. 9/25 Transistor sizing
15. 9/28 Logical effort
16. 9/30 **MIDTERM 1**
17. 10/2 Logical effort, cont'd
18. 10/5 RLC interconnect models
19. 10/7 Buffer insertion
20. 10/9 Ratioed logic
21. 10/12 Previous topic, cont'd
22. 10/14 Pass transistor logic
23. 10/16 Previous topic, cont'd
24. 10/19 Dynamic logic: Domino logic
25. 10/21 Signal integrity issues for dynamic logic
26. 10/23 Dynamic logic: np-CMOS, MODL
27. 10/26 Sequential logic circuits
28. 10/28 Static latches and registers
29. 10/30 Dynamic latches and registers
30. 11/2 Previous topic, cont'd
31. 11/4 **MIDTERM 2**
32. 11/6 Pipelining
33. 11/9 Adder designs
34. 11/11 Previous topic, cont'd
35. 11/13 Low-power design techniques
36. 11/16 Semiconductor memories
37. 11/18 Semiconductor memory: Control logic
38. 11/20 SRAM
39. 11/30 Previous topic, cont'd
40. 12/2 DRAM
41. 12/4 Previous topic, cont'd
42. 12/7 I/O circuits; Brief introduction to silicon-on-insulator (SOI)
43. 12/9 Review